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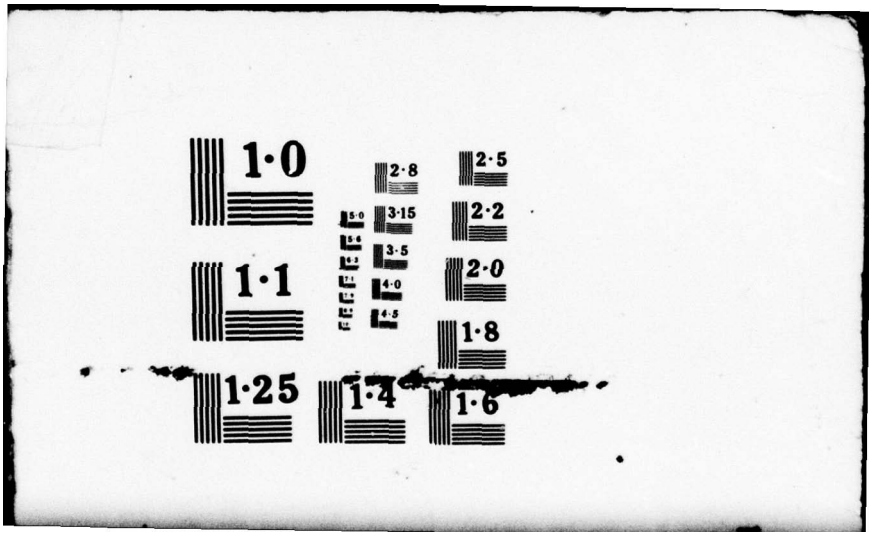
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LEVEL II

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Final Technical Report
February 1979

ELECTRICAL CHARACTERIZATION OF 16K DYNAMIC RAMs

IBM

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Electrical characterizations were performed on 16K dynamic RAMs available from the merchant semiconductor industry. Based on the data obtained, parameter limits were established and proposed for a draft 38510 specification. The data, proposed limits, and related discussion are presented.

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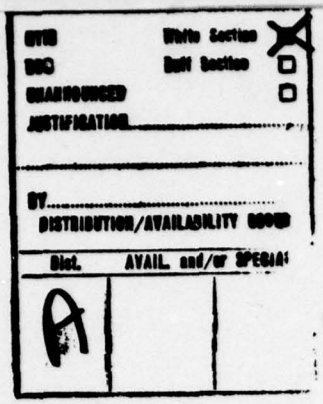

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EVALUATION

The prime objective of this study was to electrically characterize and specify in MIL-M-38510 detail specification format 16K bit dynamic random access memories (RAMs). Several different vendors' devices were to be evaluated to assure second source advantages of cost and delivery.

The specific approach to accomplish the above objectives was to perform a complete electrical characterization of 16K RAMs from the industry leader, referred to as "Vendor A" in this report. At the completion of this task other vendors' devices were to be selected and the critical electrical parameters evaluated. From the resulting data, a detailed MIL-M-38510 specification was to be prepared.

The results of this effort, as verified in this report, were successful in achieving the desired results. The 16K dynamic RAM available from at least three large semiconductor vendors was completely characterized and specified in MIL-M-38510 format. In fact, the resulting specification, nomenclatured M38510/240, was issued, coordinated and dated during the course of this contract.

This specification contains a comprehensive list of a-c and d-c parameters along with algorithmic test patterns needed to assure the electrical integrity of 16K dynamic RAMs. Critical tests peculiar to 16K dynamic RAMs, such as the "bump test" to guarantee sense amplifier performance are contained in this specification. Alpha particle emission from the packaging materials that can cause soft memory errors is also treated in this specification as an initial attempt at quantifying the effects of the problem in system operation. Future studies of the effects in alpha particles on dynamic RAMs will be pursued at RADC.

RADC, as preparing activity of MIL-M-38510, is responsible for managing the development and preparation of detail slash sheets for this specification. This study and future studies of this type will be contined to assure that the MIL-M-38510 detail specifications are electrically accurate, cost effective, timely and capable of guaranteeing that microcircuits will perform as specified in design applications.

Regis C. Hilow

REGIS C. HILOW
Project Engineer

1.0 INTRODUCTION

The evolution of the 16K dynamic RAM is a result of one of the keenest concerted efforts by the semiconductor memory industry to date to provide the user base with a standard form, fit, and function memory device. The primary reason for its immediate acceptance by the user was its basic functional concept. With this functional concept well defined, the semiconductor industry was both ready and capable of producing such a high density device. Since its introduction in early 1976, capabilities such as a mature double polysilicon process and a complete menu of third-generation dynamic circuit techniques have come together throughout a broad segment of the industry to provide the user with the most attractive cost/performance memory technology to date.

The wide temperature range performance inherent in most designs has made it possible for the government to be offered these same cost/performance advantages in many main store applications. With this in mind, IBM Federal Systems Division (FSD) has performed electrical characterizations on 16K dynamic RAMs for this purpose. As a separate but related data item, a draft of the MIL-M-38510/240 military specification for the 16K dynamic RAM was prepared and submitted to RADC as part of this project.

This final report is comprised of a large quantity of reduced data which justifies the limits set forth in the proposed draft specification. It is hoped that it will serve as a comparison reference manual for future product designs and revisions.

The explanation of the operation of the 16K dynamic RAM is covered in numerous data books, articles, and application notes and will not be repeated in this report. Lengthy comments and wording are also minimized.

2.0 OBJECTIVES OF THE PROJECT

The objectives of the project were as follows:

1. Characterize a popular version of a 16K RAM for the purpose of establishing draft specification limits.

2. Demonstrate on a "best effort" basis that alternate devices made by more than one vendor are interchangeable on a pin and performance basis.

3. Generate a draft 38510 slash sheet specification for the 16K RAM using characterization data as a basis for establishing performance limits.

3.0 CONCLUSIONS

All objectives of the project were met or exceeded. With respect to "device interchangeability" aspects, reduced effort characterizations were performed during a two-month time window (April through May 1978). Therefore, for those vendors whose "production runner" was not available during that period, only a limited amount of data, consisting of highlight parameters (i.e., t_{RAC}, I_{DD1}, etc.), was collected on those particular devices.

It has been concluded that companies in the merchant semiconductor industry can supply a 16K dynamic RAM that will operate over the temperature range of -55°C case (instant on) to +110°C case (operating) with an access/cycle time of 200 NS MAX/375 NS MIN, a power supply tolerance of ±10 percent, and a retention time of 1.0 MS minimum.

The data presented in Appendices I (Vendor A), II (Vendor B), III (Vendor C), and IV (Parameter Comparison Plots) are the basis for the conclusion. The recommended limits for all parameters are given in Appendix V (Recommended Parameter Limits).

Examination of the input high level data shows that the 2.7 V MIN generally specified by data sheets can safely be lowered to 2.4 V MIN which permits the device to be truly TTL compatible on all inputs. All three vendors, whose data is shown in the appendices, have subsequently agreed to the 2.4 V MIN up level for all inputs.

Cell retention time, one of the main concerns, is not a significant yield detractor at 110°C case temperature. The data shows that only a few of the samples did not meet the 1.0 MS MIN limit. With further process improvements and circuit adjustments, particularly those intended to reduce the device's vulnerability to alpha particle induced soft errors, should minimize the data retention time issue. The reasons for this improvement is discussed in section 5.0 in greater detail.

It is genuinely felt that the parameter limits set forth in Appendix V, with minor exceptions, will satisfy the majority of users and suppliers. Device interchangeability by several different sources is clearly demonstrated in Appendix IV.

4.0 PROFILE OF A 16K DYNAMIC RAM

In advance of describing the approach for achieving the objectives, it is perhaps best to give some perspective to the device being addressed by this project. The following table illustrates some aspects of the process, design, performance, and packaging. The entries, which consist of data accumulated over one year, are still changing, particularly in light of the recent alpha particle soft error discovery.

16K DYNAMIC RAM PROFILE

	Range	Most Common
Number of U. S. Vendors	9	N/A
Ground Rules	4-6μ	5μ
Oxide Thickness	800-1000 Å	850 Å
Diffusion Depth	0.7-1.2μ	1.2μ
Die Size	22-34K mil^2	23K mil^2
Array/Chip Area Ratio	~42-50%	~50%
Cell/Bit Line Ratio	1/9-1/20	1/18
Cell Capacitance	0.032-0.080 PF	0.05 PF
Data Matrices	2-4	2
Number of Sense Amps	128-256	128
Sense Amps	Static-Dynamic	Dynamic
Access (t_{RAC})/Cycle	150-300/320-410 NS	200/375 NS
Operate/Standby Power (typ)	260-385/6-20 MW	300/12 MW
Supply Voltages	+12V,+5V,-5V $\pm$ 10%	Same
Packages	16 PIN DIP/FP or 18 PIN carrier modules consisting of stacked DIPS or multiple carriers on a pinned substrate are also available.	

Common to all these designs is the use of metal word lines and diffused bit lines, unlike at least one Japanese version where the opposite is true. Buried contacts are used extensively, and in some cases, second level poly has been used in the peripheral support circuits.

There is little variation in the one-device double polysilicon cell structure. Most are fabricated with six or seven mask NMOS processes.

From a circuit standpoint, at least one manufacturer uses static sense amplifiers and 4-storage matrices. This arrangement uses 256 sense amplifiers with 32 cells on each of the balanced bit lines. A large sensing margin is achieved partially due to the low bit line to cell capacitance ratio allowing more freedom in setting the value of the sense amp trip point. Much more common is the 128-dynamic sense amp scheme which incorporates 64 cells on each bit line half. Although the high bit line to cell capacitance ratio reduces the signal swing, present day designs have, in the process of reducing susceptability to alpha particle induced soft errors, made process changes that tend to increase the cell capacitance as well as store a much higher signal on it. The resulting high signal swing also gives some added freedom for choosing the trip point of the sense amplifier. For both the static and dynamic versions, the large signal swings have allowed for trip point settings which result in an "apparent" data retention time improvement.

The input circuits (except clocks), shown in Figure 1, are comprised of latches having a signal input and a reference input and an associated holding capacitor for each. The holding capacitors are gated off immediately after $\overline{RAS}$ or $\overline{CAS}$ becomes active so that the latch may progress in a changing state while the input signals are changing

to a new value. In some cases, a common mode boost signal is applied to the gates of both sides of the input latch to ensure that the correct side turns on.

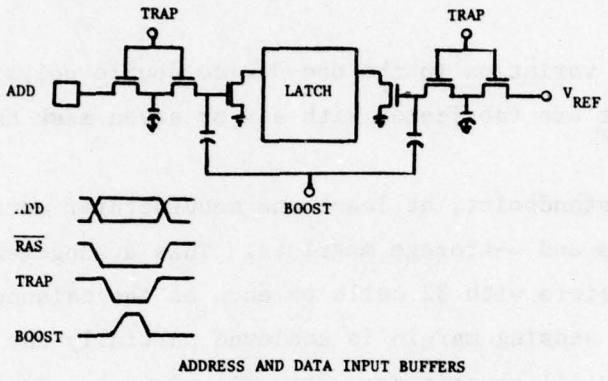


Figure 1

Input level compatability with TTL circuits for all inputs including clocks is now guaranteed and advertised by many suppliers.

The clock inputs are slight modifications of a standard boot strapped inverter which does account for nearly all the standby power consumption of the device except in those cases where static sense amplifiers are employed. Since the bulk of the operating power is dynamic, it is a direct function of frequency and the duration of the active $\overline{RAS}$ time. As a result, some devices having a high component of static power may meet a specification for a given cycle time and $\overline{RAS}$ active time, but when used in an application where the $\overline{RAS}$ active time to cycle time ratio approaches one, the power dissipation could become many times that of a fully dynamic part and for that particular application could not be considered interchangeable with it.

Data retention time is 10 to 20 times better than that exhibited by early versions of the 16K RAM. This is due, in part, to higher signal swings and lower sense amp trip point values. Other improvements such as diffused guard rings around the periphery of the storage matrix and improved gettering have reduced cell leakage currents.

From the author's viewpoint, the most impressive section of the RAM design is the control timing generator. Over 20 precisely timed control signals, some that operate twice each cycle, are developed to synchronize the orderly sequence of events. It is the generator that provides the dynamics for the dynamic RAM.

Finally, since the operating basis for the dynamic RAM amounts essentially to the charging and discharging of capacitors, which accounts for very low power per bit, the profile of the power supply current waveforms demand that good high frequency decoupling in moderate to large amounts be placed strategically throughout the second level assembly for the VDD (+12V) and VBB (-5V) supplies.

5.0 CHARACTERIZATION APPROACH

5.1 RATIONALE

The philosophy established at the outset of the projects was to arrive at a set of specification limits that were both attractive to a user and deliverable by the industry with very little added in the way of special electrical tests. Rather than testing a large number of samples from one vendor, the assets were used to collect data from fewer samples representing several suppliers instead.

This philosophy had proven to be the correct one considering the frequent number of design tweaks and die shrinks that have occurred during the span of the project.

For a reasonable given set of constraints, it is not possible or even desirable to characterize indefinitely the large number of design variations from every supplier. During the last quarter of 1977, a quick snapshot view of devices from the industry (nine United States manufacturers) showed that although all had a good set of goals and plans, the individual designs showed varying degrees of maturity. The strengths and weaknesses of many of the designs could definitely be seen at that time. The original plan of choosing one of the most stable and popular designs for a full characterization was implemented with the intent of looking at designs from other manufacturers at a later date when prospects would be better for getting production versions.

Following the above course led to the full characterization of devices from Vendor A (see Appendix I). Subsequent characterizations of Vendors B and C were also performed (see Appendices II and III). The highlight parameters are plotted and shown in Appendix IV.

In order to give some perspective to the project in relation to the production ramp-up of the 16K RAM, the following is offered. Approximately nine months after the outset of the project, the list of nine United States manufacturers has grown to eleven. According to Dataquest estimates (July 14, 1978, Dataquest newsletter), only three of these United States companies are shipping at a rate of 500K or more units per quarter, five are shipping 50K units per quarter, and the remaining are still in the sampling stage.

The foregoing illustrates that although the 16K RAM is a viable product, many changes and much "learning" is still taking place within the industry. New processes or designs aimed at reducing alpha particle vulnerability is also proliferating the number of devices that are available to consider. The overall point, re-emphasized, is that the characterizations performed were done with the intent of determining mutually reasonable specification limits for the purpose of providing the government with a draft document for procuring devices on a timely basis from more than one source at a reasonable cost and minimum procurement risk. No attempt was made to establish binning criteria or parameter distribution for any vendor's product.

5.2 TEMPERATURE RATIONALE

Because the most important parameter of a dynamic RAM, data retention time, is a strong function of temperature (halving every 5-20^{o}C), the previously accepted but vague concept of ambient temperature is not acceptable for characterization purposes. There is a wide variation of conditions for specifying as well as for interpreting the meaning of this term. In system thermal definition and analysis, it is not a usable parameter. In some military high-altitude applications, for example, there is no "air," still or moving, demonstrating the inadequacy of the standard "ambient" temperature specification. Even in commercial applications, the temperature environment is usually modified by fans or heat sinks or other conduction methods all of which require a more accurate method for specifying device temperature.

As a better choice, junction temperature seems at first to be more useful since junction-to-case thermal resistance has been measured and calculated and is related only to the properties and dimensions of the chip and package. However, one is sometimes faced with the problem of defining just where and at what temperature the precise junction is. To date, direct measurement of temperature at the precise junction locations has not been practical, although temperatures in the "junction vicinity" have. Models have been developed to calculate precise junction temperatures but cannot be experimentally verified. Therefore, to circumvent this age old problem, of which the author is well aware, a more practical concept has been set forth, one that is suitable for engineering or production environments.

For the purpose of this project, junction temperature is defined as the average bulk temperature of the silicon chip. This is an easily acceptable definition if it is remembered that in memory devices the power is dissipated quite evenly accross the chip. In this particular case, the 16K RAM device chip temperature was measured with an infrared radiometric microscope while the chip was being sequentially addressed at a 375 NS cycle rate. The resultant "junction" to case thermal resistance was three to five degrees C per watt referenced to the bottom side center of the 16 pin DIP. This number was verified on two radiometer setups and was subsequently verified by one device vendor.

Further, it is realized that this method as well as others could be considered controversial or not acceptable by some; however, it was used to estimate junction temperatures in this characterization and has proven to be usable. To further remove any ambiguity, it was

decided to specify the device temperature range in terms of case temperature measured at the bottom center of the DIP. In addition, the junction-to-case thermal resistance is specified at 15°C/watt maximum (three times the measured value) to account for measurement variations. Within this framework, the junction temperature for electrical or reliability concerns is considered to be less than 7°C above the case temperature at cycle times of 375 NS.

5.3 TMEPERATURE FIXTURING

The temperature forcing system used for the entire range of -55°C to +110°C case was a Temptronic hot probe (Model TP 26/27H) and cold probe (Model TP 27C). Temperature measurements were made with a Digitec Thermocouple Thermometer (Model 590 TC Type T). A 20-mil diameter copper constantan thermocouple was attached to the device socket with a small piece of low emissivity tape.

The thermocouple is an averaging device and therefore measures the average of everything that contacts the junction bead and therefore must be calibrated to case temperature. When a thermospot forcing system is used, a hot or cold probe is brought in contact with the lid of the test package. When the hot probe is used, the heat flow is downward toward the device, socket, and card. Conversely, when the cold probe is used, the heat flow is in the opposite direction and toward the probe. Therefore, when measuring case temperature, the thermometer reading will contain a negative error when the hot probe is used and a positive error when the cold probe is used. Put another way, the actual case temperature will be higher than indicated at high temperatures and lower than indicated at low temperatures.

To quantify this error, the entire card, thermocouple, and device are put in an oven having fan-forced violent air movement. The device is unpowered, and under these conditions the case, socket, card, and entire thermocouple bead are assumed to be at the same temperature. A low current (100 UA) is passed through an input protection diode while no other power is applied to the chip. At several temperatures over the -55°C to +110°C range, both the value to the thermometer indicator and the diode voltage is plotted.

Next, with the device, socket, and thermocouple still intact, the card is transferred to the thermal probe fixture where all future characterizations will be done. Here, the calibration curve is completed by adjusting the temperature for diode voltage readings previously obtained and recording the indicated temperature. This curve is illustrated in Figure 2 below.

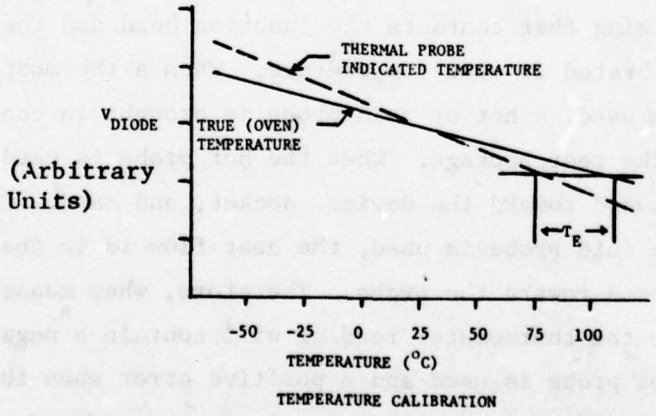


Figure 2

Referring to the illustration, the true case temperature is taken to be that measured in the oven environment. The fixturing error is the difference between the oven fixture indications and the thermal probe fixture indications. For this particular project, the error was found to be:

$$T_E = 0.04\ (T-25)^{\circ}C$$

where T = the indicated thermometer reading

where T_E = the error in the indicated thermometer reading

$$Tcase = T + T_E = T + 0.04\ (T-25)$$

$$Tcase = 1.04T - 1\ ^{\circ}C$$

The repeatability of the setup was determined to be within $0.5^{\circ}C$ at an indicated reading of $100^{\circ}C$.

5.4 MEMORY EXERCISER

The memory exerciser used for all testing was a Siemans Venture V200 geared primarily for engineering characterizations. The exerciser is equipped with a topological memory for both the X and Y address fields. All devices were tested in a topologically pure fashion using topo maps readily available from each vendor.

5.5 TEST ALGORITHMS

The test algorithms are given in Appendix VI. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory. Each algorithm serves a specific purpose. Appendix VI gives detailed

descriptions of the patterns used for device characterization. All are commonly known patterns and should be quite simple for most test systems to implement. The subject of identifying the ideal efficient pattern (i.e., minimum test time/maximum effectiveness) is not within the scope of this project. Separate studies have been performed on this subject, but it is too early to draw a conclusion based on these algorithms being used in actual production or failure analysis testing. Nonetheless, the economic importance of this subject is recognized and will be addressed in future activities.

5.6 SAMPLE SELECTION CRITERIA

One of the primary objectives of the project was to provide a set of specifications for the 16K dynamic RAM that would afford the government the same cost/performance advantages available to private industry. To assist in achieving this goal, the samples were chosen to implement the following plan:

a. Procure and test 25 commercial grade (0° to 70°C) RAMs from several vendors and determine the performance and extended temperature range capabilities <u>inherent</u> in each of the designs.

b. Fully characterize 25 samples of a popular version and follow with at least two additional versions.

c. Write a draft specification, using the characterization data base, the industry can meet with as little additional special testing as possible.

The selection of samples prescreened to any criteria other than that outlined on the previous page would have biased the outcome and made it impossible to achieve the original goal.

6.0 PRESENTATION AND EXPLANATION OF THE DATA

All electrical measurements were taken at -55°C, +25°C, and +110°C case temperature. After reduction, it was plotted to a smooth curve format so that parameter values could be lifted for other intermediate temperatures.

The AC data was plotted to a particular and useful format. All data concerning a single parameter is presented on a single page. The first plot at the top of the page shows the cumulative distribution of the sample group for that parameter. A glance at this plot shows if maverick parts exist in the sample. The second plot shows how the parameter varies with power supply voltage (V_{DD}), while the third plot illustrates how the parameter performs over the full temperature range.

Cell retention was measured at three elevated temperature points (90°C, 100°C, and 110°C case) using pattern five in Appendix VI. These plots show retention time halving every 5° to 20°C with 12°C being typical. Slopes of retention time versus temperature do not seem to be related to the absolute value at any temperature. Thus, a device having a low retention time and shallow slope initially at a given temperature might have a longer retention time than one starting with a higher initial value having a steeper slope when both are measured at a higher temperature. In any case, a 1.0 MS MIN limit at 110°C case can be met with little fallout.

Plots of output source and sink capability were made on a pulsed basis since the output is at a valid level for only a short 10 USEC interval.

TYPICAL OUTPUT RESISTANCE (OHMS)

		Vendor A	Vendor B	Vendor C
Sourcing	-55°C	98	42	46
	+25°C	126	58	66
	+110°C	159	82	93
Sinking	-55°C	21	13	16
	+25°C	31	20	26
	+110°C	44	29	38

An empirically derived equation for calculating standby and operating current is shown in Appendix I for Vendor A. Some published equations are derived from a slope of I_{DD1} vs frequency where the intercept of the current axis for $\overline{RAS}$ and $\overline{CAS}$ is active when the frequency is zero. In a system design, this would not usually be the case, as one would normally make $\overline{CAS}$ and $\overline{RAS}$ inactive for this condition. In very large systems, this seemingly minor error could have a heavy impact on the choice of the power regulators. The equation shown is included to serve only as an example.

The last set of plots for each vendor show the V_{DD} vs V_{BB} schmoos. These schmoos indicate a large margin of operation for supply voltages. Both a 5% and a 10% "box" are shown. For the characterization, the V_{BB} power supply was limited to -7.0 V maximum and the V_{DD} supply was limited to 15.0 V maximum to remove the possibility

of accidentally exceeding the maximum 22.0 V breakdown limit since the sample size was small. The only notable point is that the left edge of the schmoos are different--Vendor A is rather abrupt while Vendor B is more rounded. Vendor B plots also show wide variation in V_{BB} dependency from device to device, but since schmoo boundries are generally determined by a relatively few number of cells on the chip, no great significance can be attached to that behavior, particularly if the tight schmoo (Unit #8) is not a trend.

Appendix IV, Parameter Comparison Plots, is included as a convenient comparison of the highlight parameters (t_{RAC}, t_{CAC}, I_{DD1}, etc.). The dotted lines on the plot indicate the proposed spec limit for that parameter. The intent here is to demonstrate to a high degree that the devices are interchangeable for all the proposed limits. To this end also, a memory system was populated with a mixture of devices from the three vendors and has operated over the full -55^{o} to $+110^{o}C$ environment.

Appendix V is a list of the 39 AC and 19 DC proposed paramter limits that reflect the results of the data obtained from all of the characterizations.

APPENDIX I

16K DYNAMIC RAM

VENDOR A

Vendor: A
P/N:
REV: G
Date Code: 7751
Devices: 25

16K DYNAMIC RAM

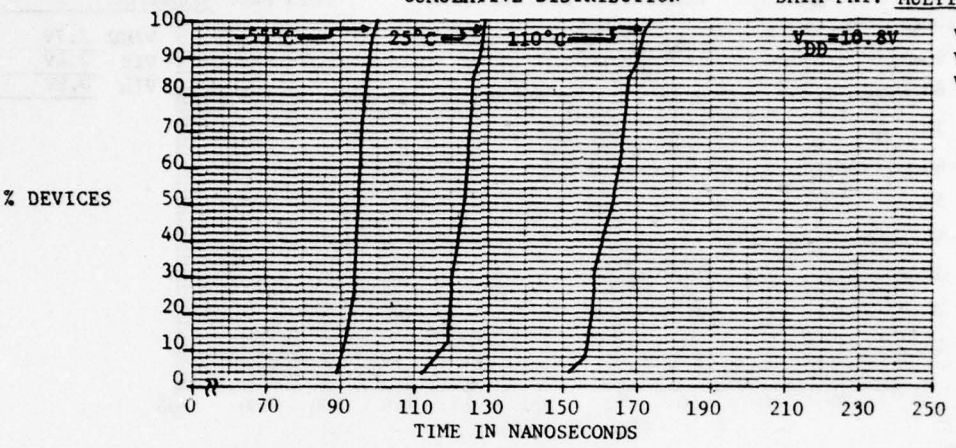
ACCESS TIME FROM $\overline{RAS}$

t_{RAC}

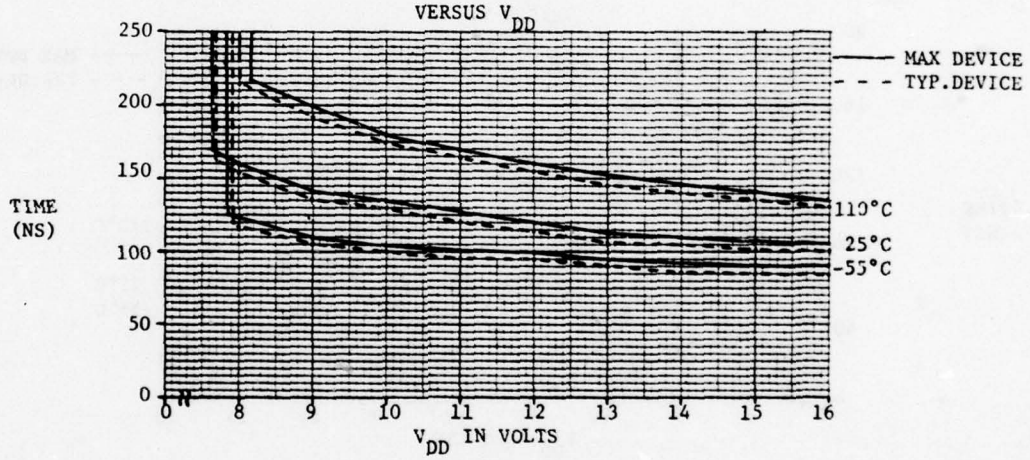
CUMULATIVE DISTRIBUTION

By F.A.N. Date 12/28/77
V_{BB} -5.0V V_{CC} 5.0V
LOAD 1 SCHOTTKY TTL + 50pF
ADDR PAT. MULTIPLE
DATA PAT. MULTIPLE

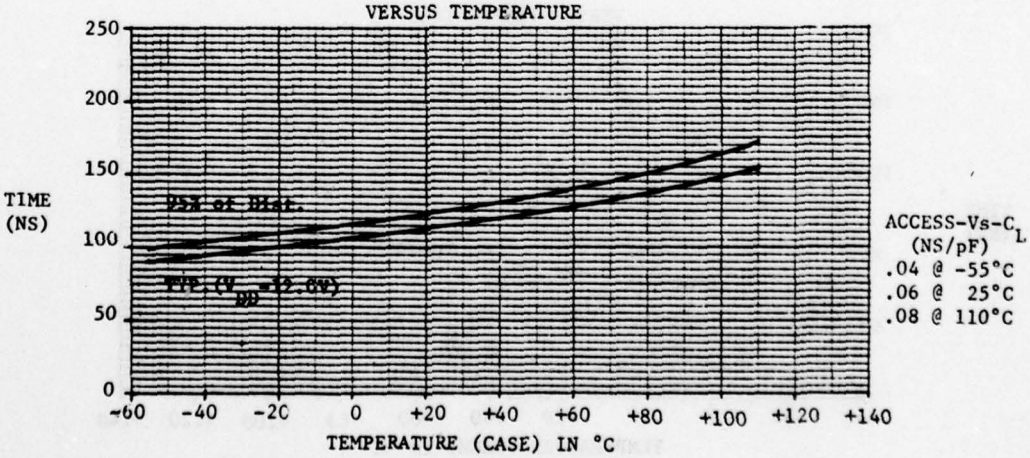
VIHC 2.7V
VIH 2.4V
VIL 0.8V



VERSUS V_{DD}



VERSUS TEMPERATURE



ACCESS-Vs-C_L (NS/pF)
.04 @ -55°C
.06 @ 25°C
.08 @ 110°C

Vendor: A
P/N:
REV: G
Date Code: 7751
Device: 25

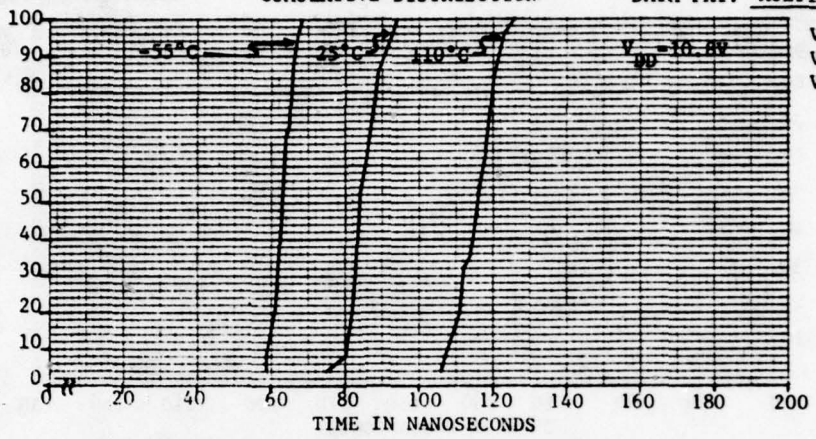
16K DYNAMIC RAM

ACCESS TIME FROM $\overline{CAS}$

t_{CAC}

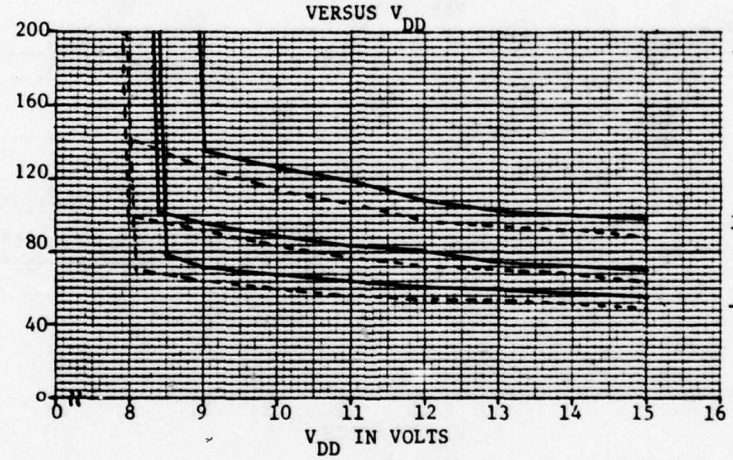
By F.A.N. Date 12/29/77
V_{BB} -5.0V V_{CC} 5.0V
LOAD 1 SCHOTTKY TTL +50pF
ADDR PAT. MULTIPLE
DATA PAT. MULTIPLE

CUMULATIVE DISTRIBUTION

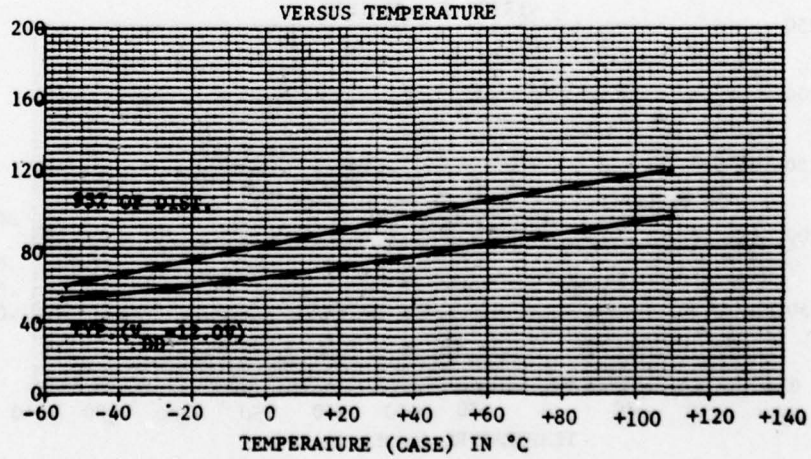


VIHC 2.7V
VIH 2.4V
VIL 0.8V

VERSUS V_{DD}



VERSUS TEMPERATURE



Vendor: A
P/N:
REV: G
Date Code: 7751
Device: 25

16K DYNAMIC RAM

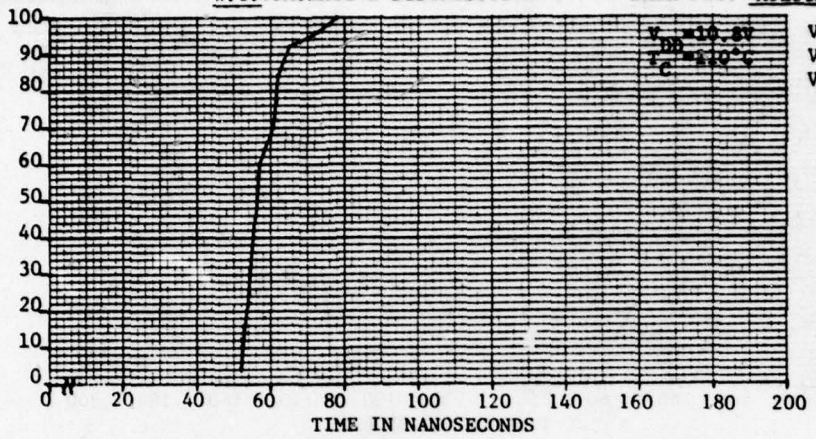
RAS PRECHARGE TIME

t_{RP}

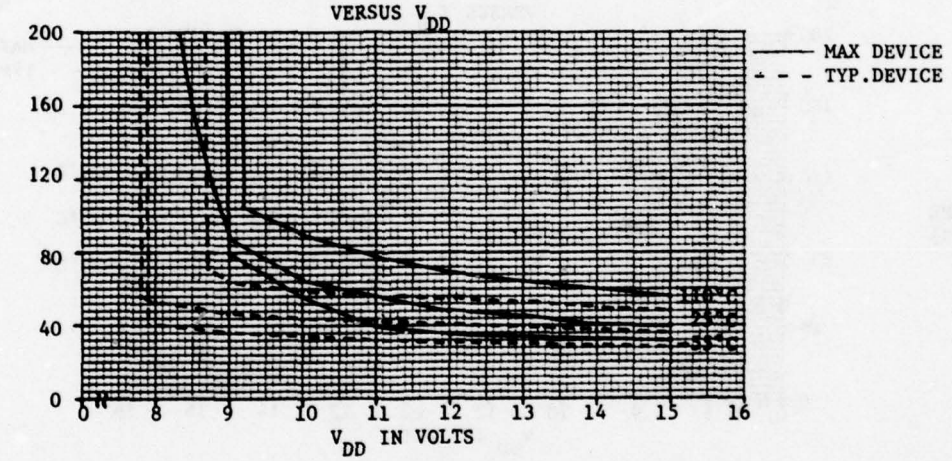
By J.R.F. Date 1/19/78
V_{BB} -4.5V V_{CC} 5.0V
LOAD N.A.
ADDR PAT. MULTIPLE
DATA PAT. MULTIPLE

VIHC 2.7V
VIH 2.4V
VIL 0.8V

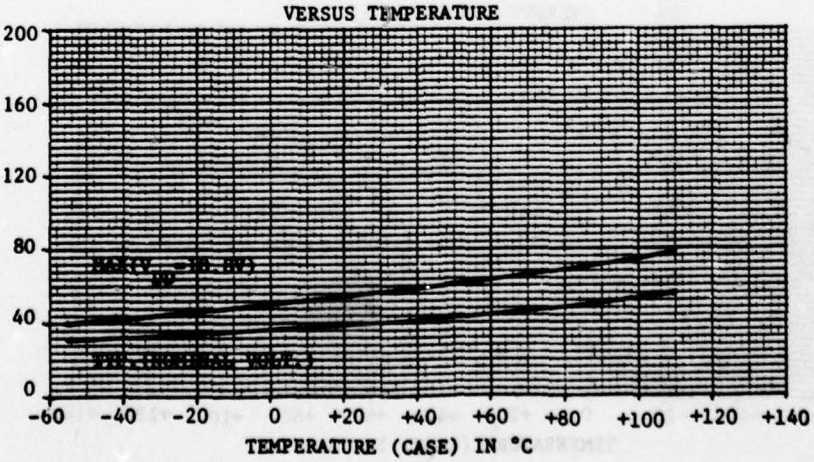
W.C.CUMULATIVE DISTRIBUTION



VERSUS V_{DD}



VERSUS TEMPERATURE



Vendor: A
P/N:
REV: G
Date Code: 7751
Device: 25

16K DYNAMIC RAM

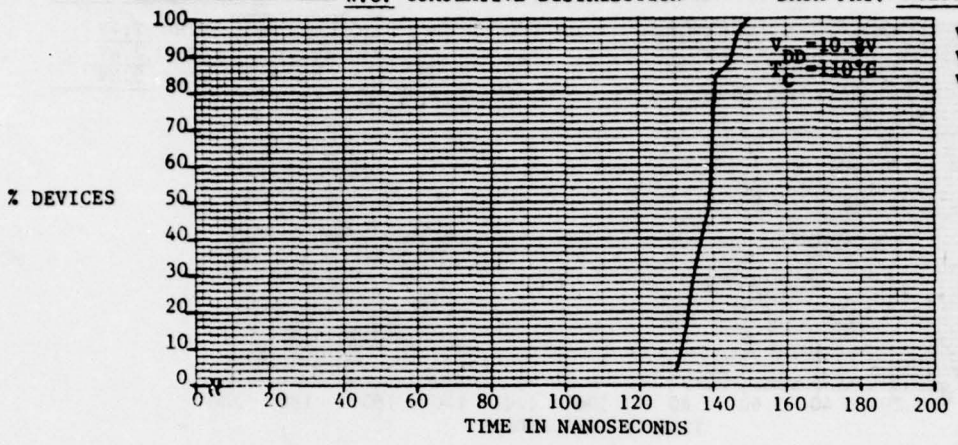
MINIMUM $\overline{RAS}$ PULSE WIDTH

t_{RAS}

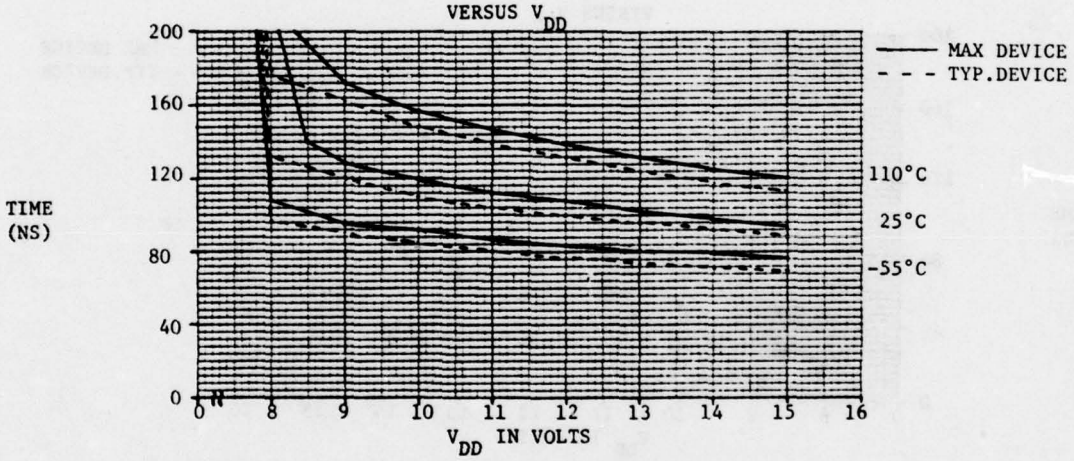
W.C. CUMULATIVE DISTRIBUTION

By J.R.F. Date 1/19/78
V_{BB} -4.5V V_{CC} 5.0V
LOAD N.A.
ADDR PAT. MULTIPLE
DATA PAT. MULTIPLE

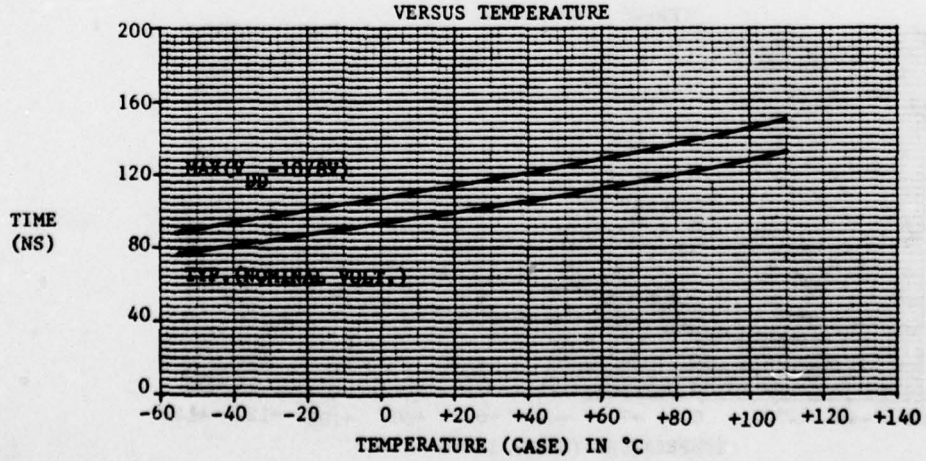
VIHC 2.7V
VIH 2.4V
VIL 0.8V



VERSUS V_{DD}



VERSUS TEMPERATURE



Vendor: A
P/N:
REV: G
Date Code: 7751
Devices: 25

16K DYNAMIC RAM

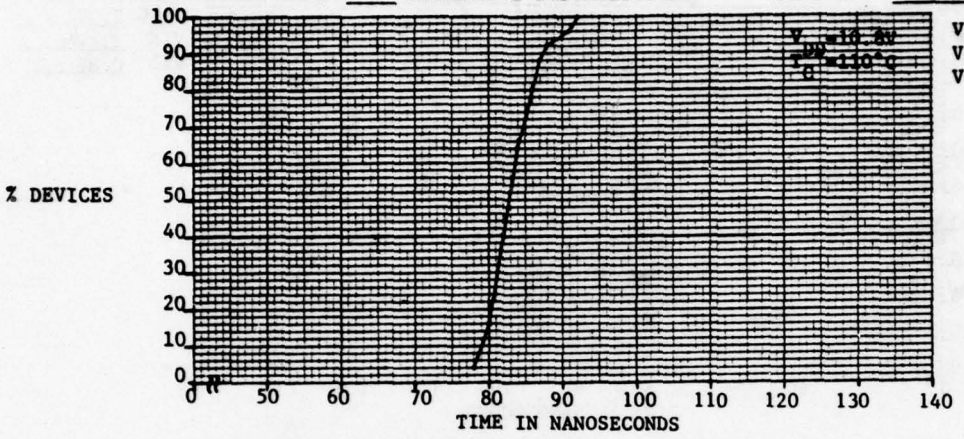
RAS HOLD TIME

t_{RSH}

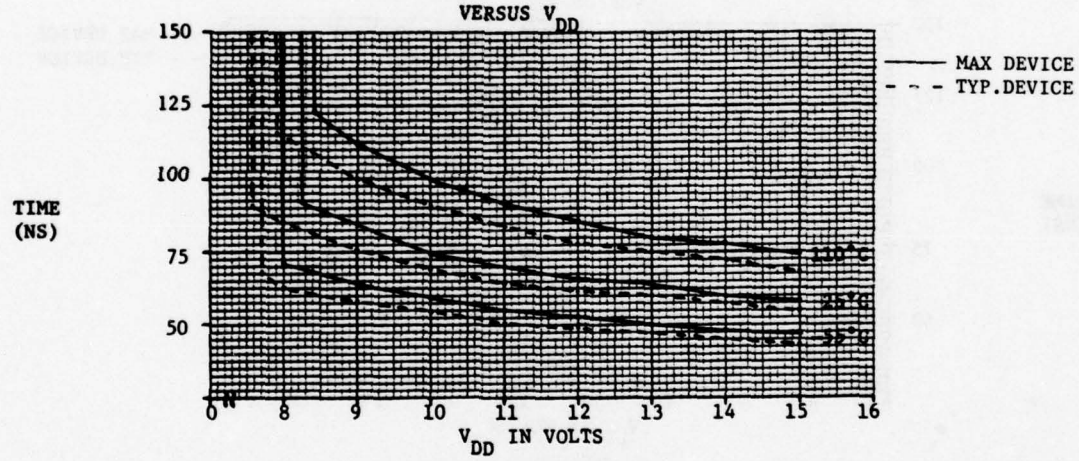
W.C. CUMULATIVE DISTRIBUTION

By J.R.F. Date 1/20/78
V_{BB} -4.5V V_{CC} 5.0V
LOAD N.A.
ADDR PAT. MULTIPLE
DATA PAT. MULTIPLE

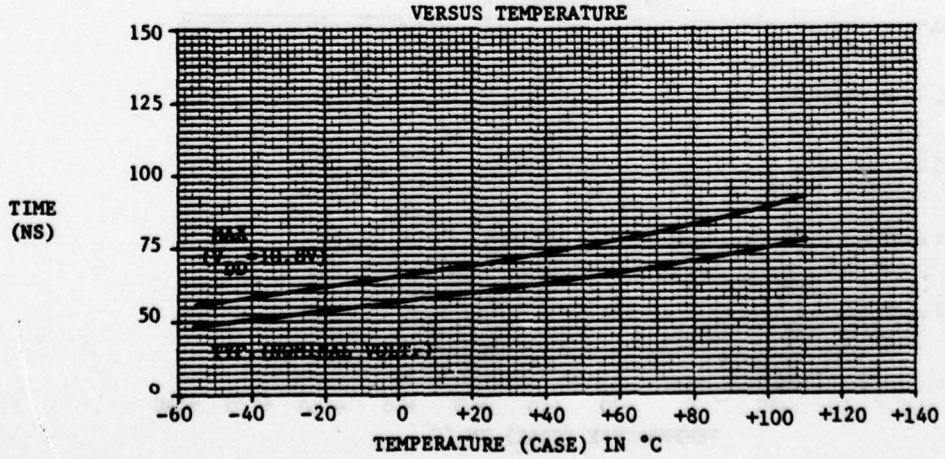
VIHC 2.7V
VIH 2.4V
VIL 0.8V



VERSUS V_{DD}



VERSUS TEMPERATURE



Vendor: A
P/N:
REV: G
Date Code: 7751
Devices: 25

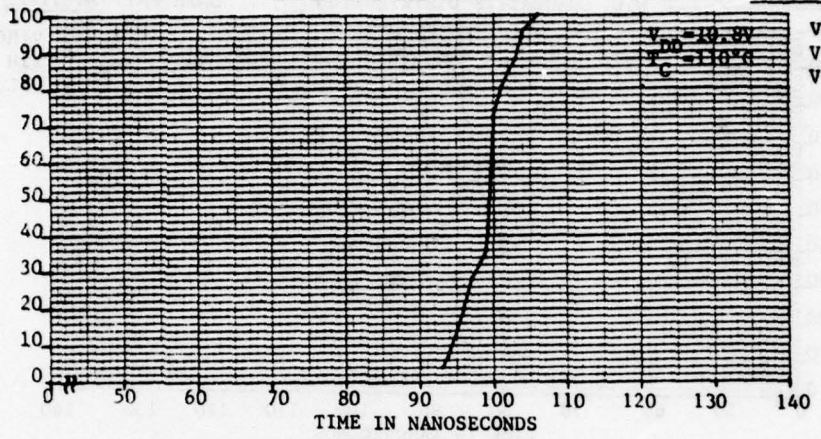
16K DYNAMIC RAM

MINIMUM $\overline{CAS}$ PULSE WIDTH

t_{CAS}

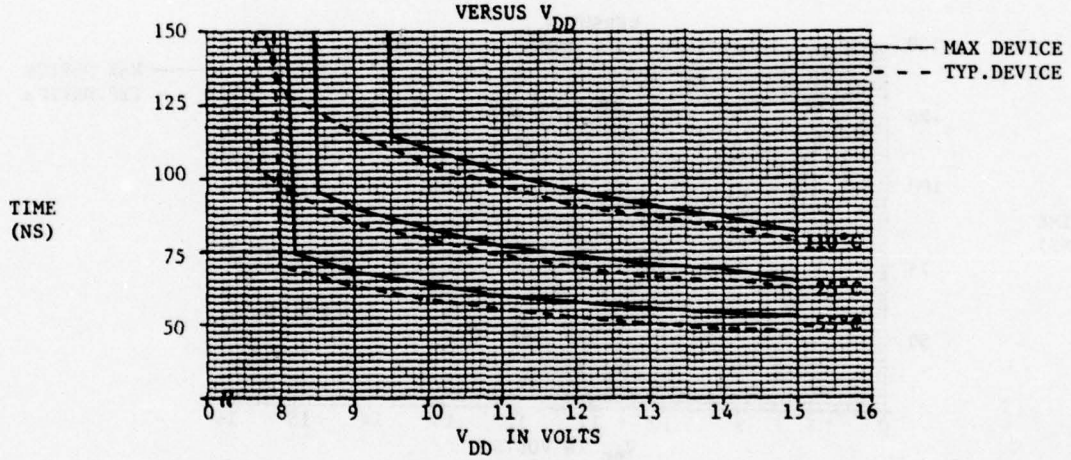
CUMULATIVE DISTRIBUTION

By J.R.F. Date 1/23/78
V_{BB} -4.5V V_{CC} 5.0V
LOAD N.A.
ADDR PAT. MULTIPLE
DATA PAT. MULTIPLE

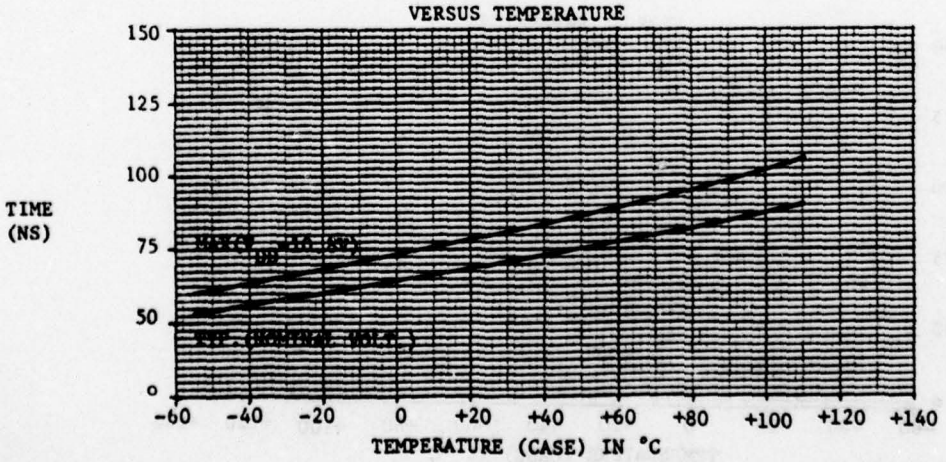


VIHC 2.7V
VIH 2.4V
VIL 0.8V

VERSUS V_{DD}



VERSUS TEMPERATURE



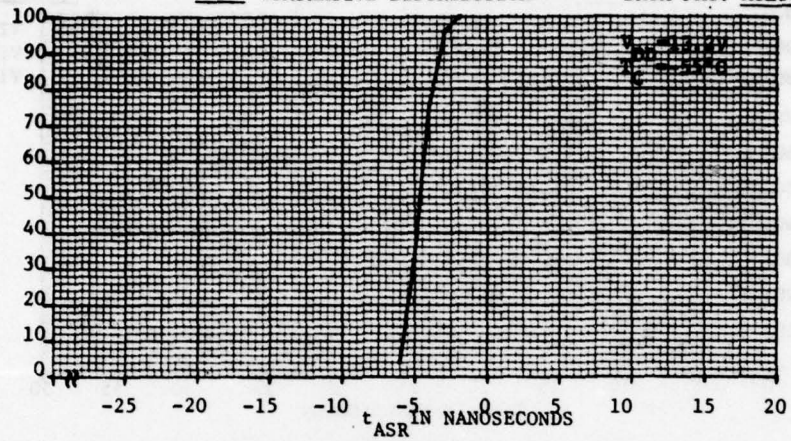
Vendor: A
P/N:
REV: G
Date Code: 7751
Devices 25

16K DYNAMIC RAM
ROW ADDRESS SETUP TIME
t_{ASR}

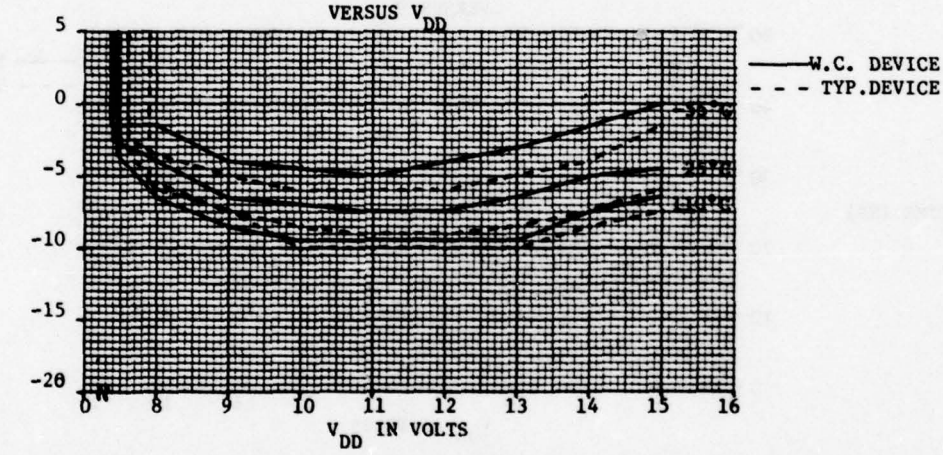
By J.F.&F.N. Date 1/24/78
V_{BB} -5.5V V_{CC} 5.0V
LOAD N.A.
ADDR PAT. MULTIPLE
DATA PAT. MULTIPLE

W.C. CUMULATIVE DISTRIBUTION

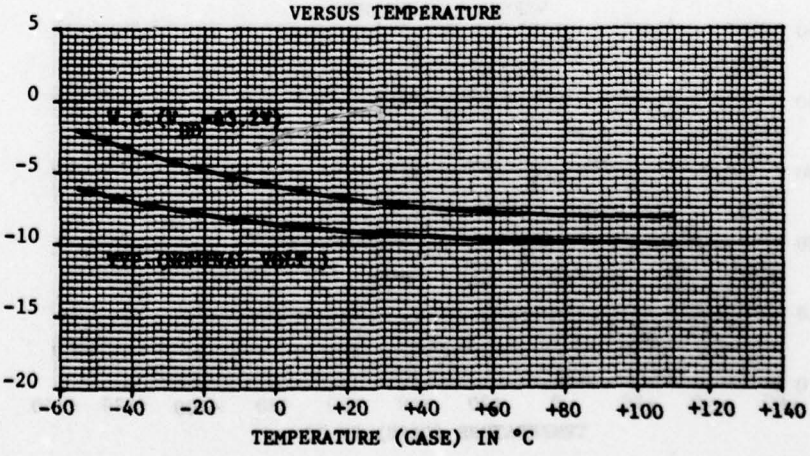
VIHC 2.7V
VIH 2.4V
VIL 0.8V



VERSUS V_{DD}



VERSUS TEMPERATURE

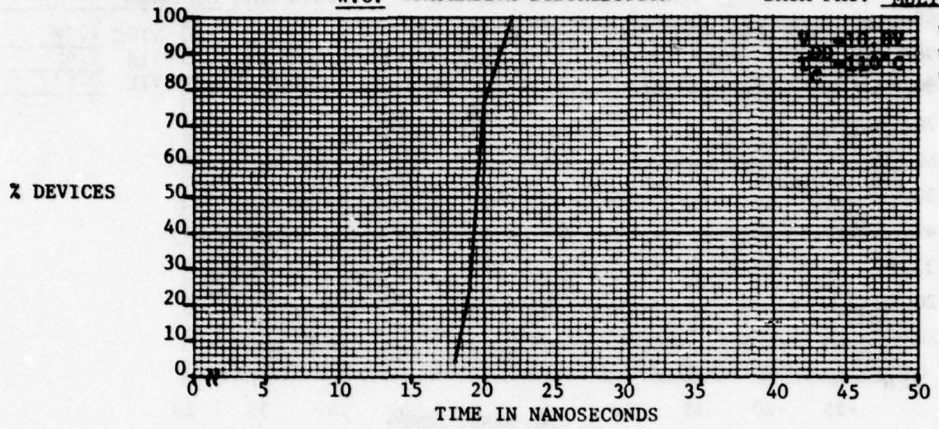


Vendor: A
P/N:
REV: G
Date Code: 7751
DEVICES 25

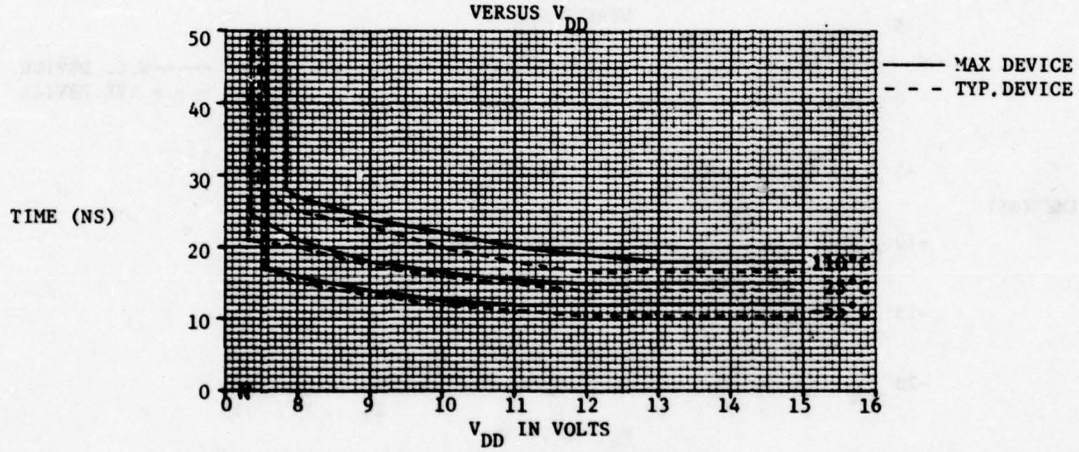
16K DYNAMIC RAM
ROW ADDRESS HOLD TIME
t_{RAH}
W.C. CUMULATIVE DISTRIBUTION

By J.F.& F.N. Date 1/24/78
V_{BB} -4.5V V_{CC} 5.0V
LOAD N.A.
ADDR PAT. MULTIPLE
DATA PAT. MULTIPLE

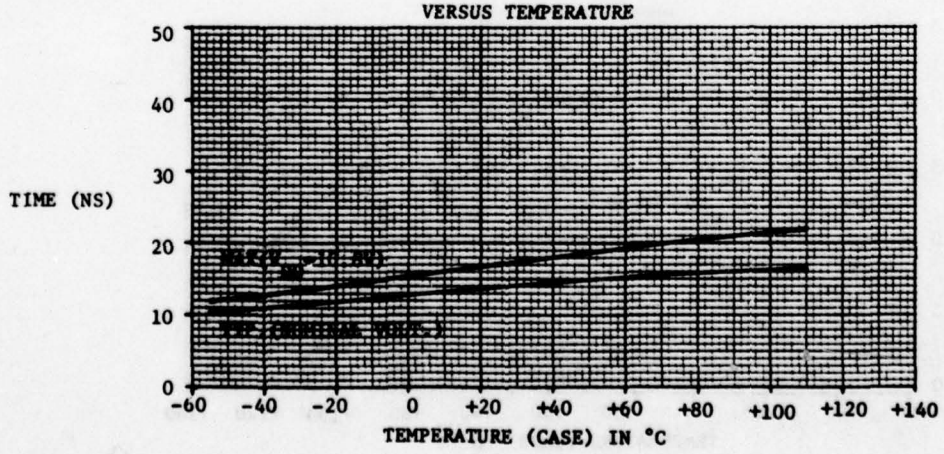
VIHC 2.7V
VIH 2.4V
VIL 0.8V



VERSUS V_{DD}



VERSUS TEMPERATURE



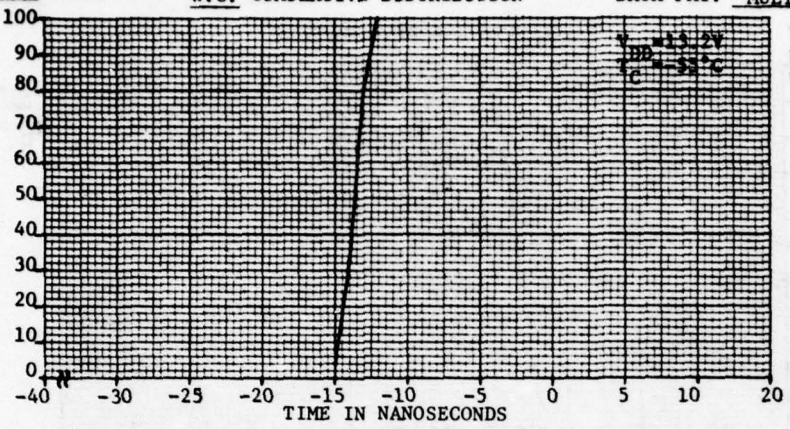
Vendor: A
P/N:
REV: G
Date Code: 7751
DEVICES 25

16K DYNAMIC RAM
COLUMN ADDRESS SETUP TIME
t_{ASC}

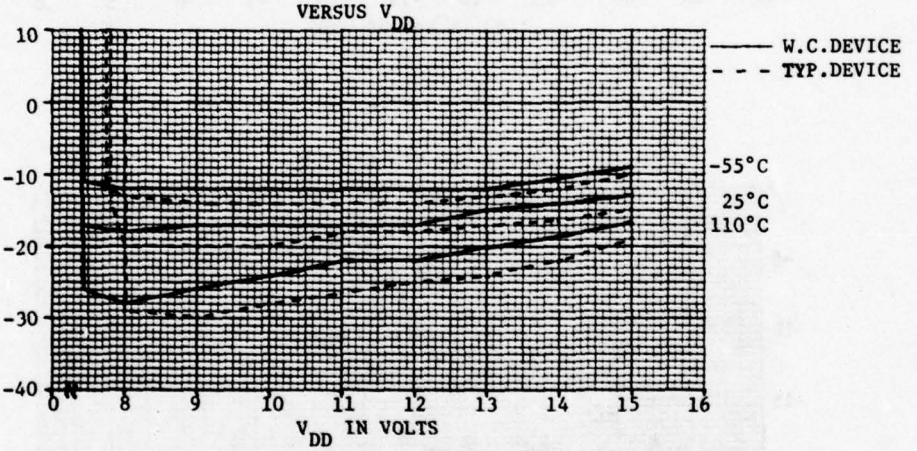
By J.F.& F.N. Date 1/25/78
V_{BB} -5.5V V_{CC} 5.0V
LOAD N.A.
ADDR PAT. MULTIPLE
DATA PAT. MULTIPLE

W.C. CUMULATIVE DISTRIBUTION

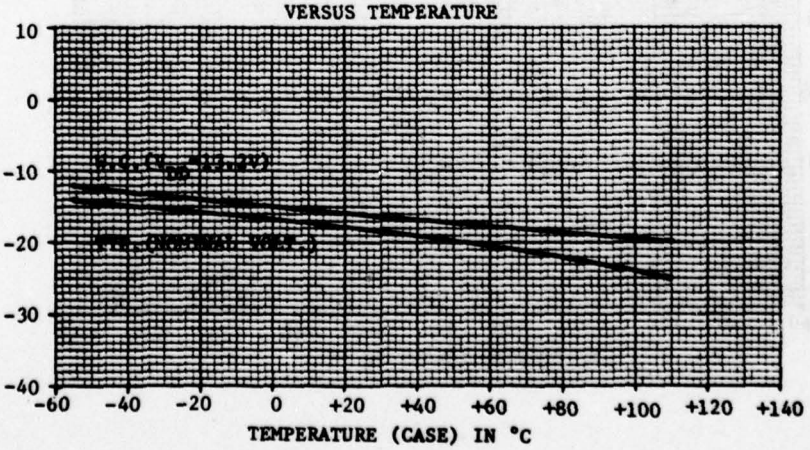
VIHC 2.7V
VIH 2.4V
VIL 0.8V



VERSUS V_{DD}



VERSUS TEMPERATURE

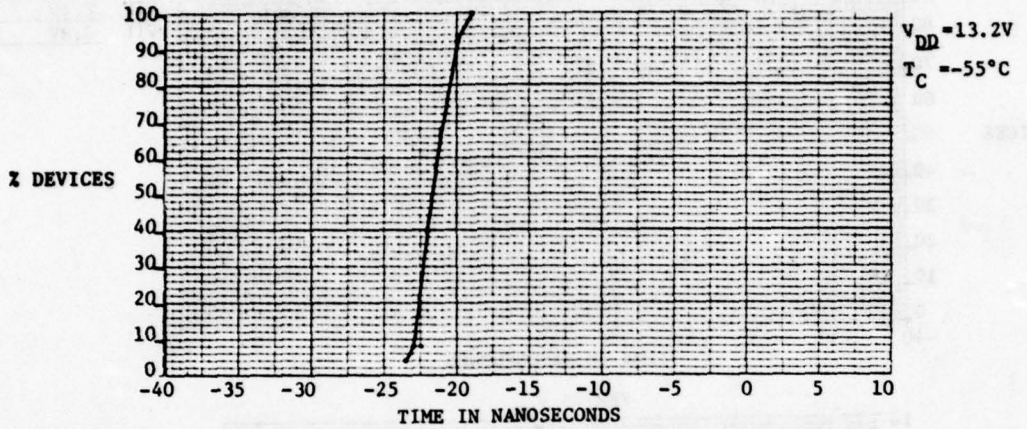


Vendor: A
P/N:
REV: G
Date Code: 7751
DEVICES 25

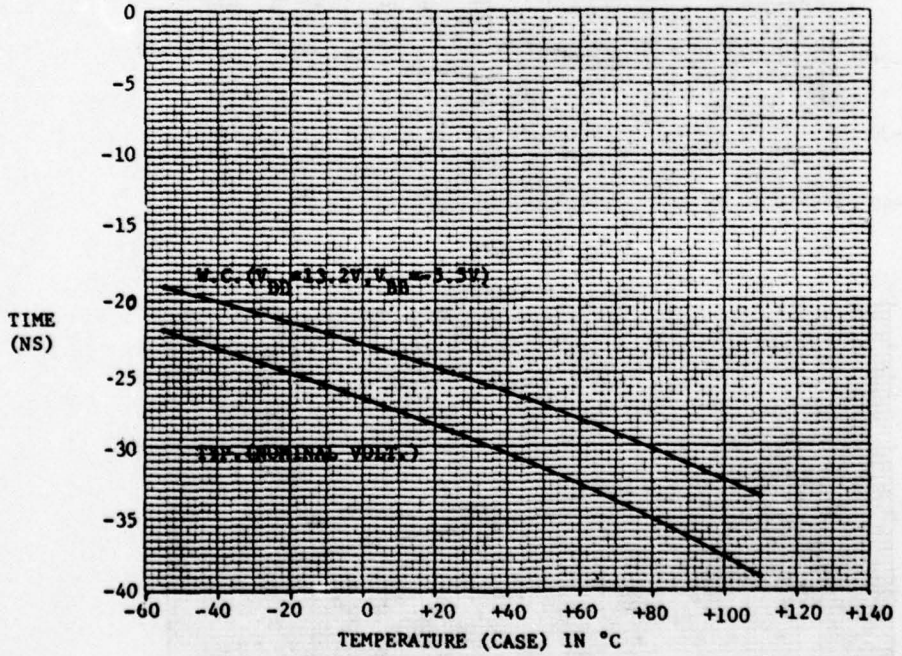
16K DYNAMIC RAM
READ COMMAND SET-UP TIME
t_{RCS}

By J.F.& F.N. Date 2/10/78
V_{BB} -5.5V V_{CC} 5.0V
LOAD N.A.
ADDR PAT. MULTIPLE
DATA PAT. MULTIPLE

W.C. CUMULATIVE DISTRIBUTION



VERSUS TEMPERATURE



Vendor: A
P/N:
REV: G
Date Code: 7751
#DEVICES 25

16K DYNAMIC RAM

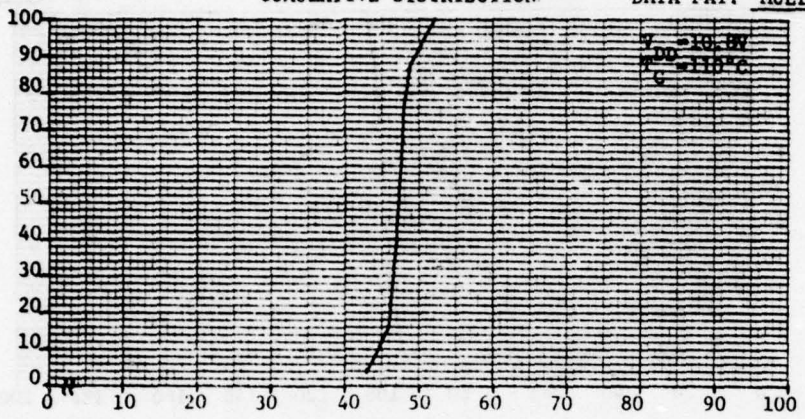
WRITE COMMAND HOLD TIME TO $\overline{CAS}$

t_{WCH}

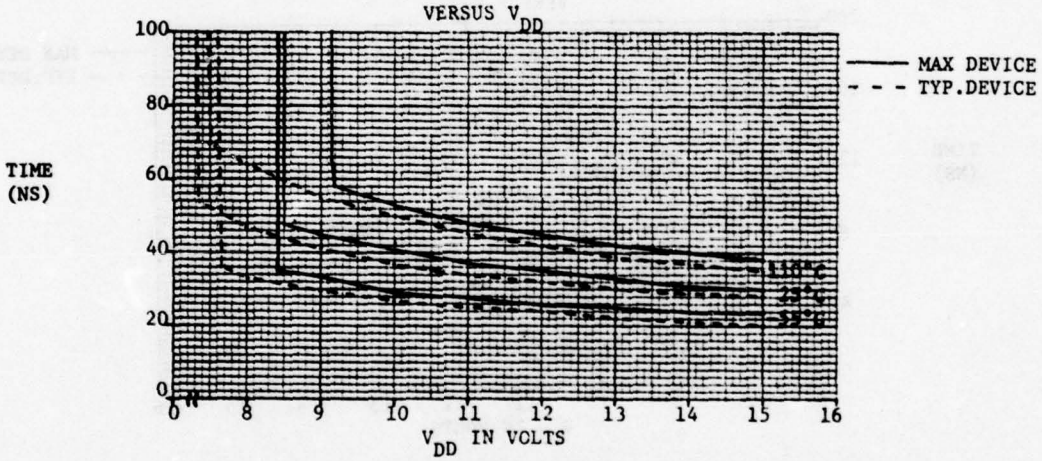
CUMULATIVE DISTRIBUTION

By J.F.& F.N. Date 1/27/78
V_{BB} -4.5V V_{CC} 5.0V
LOAD N.A.
ADDR PAT. MULTIPLE
DATA PAT. MULTIPLE

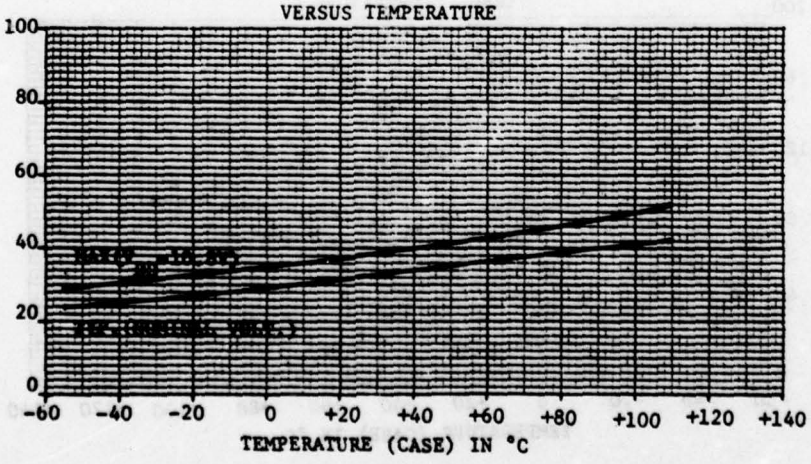
VIHC 2.7V
VIH 2.4V
VIL 0.8V



VERSUS V_{DD}



VERSUS TEMPERATURE



Vendor: A
P/N:
REV: G
Date Code: 7751
DEVICES 25

16K DYNAMIC RAM

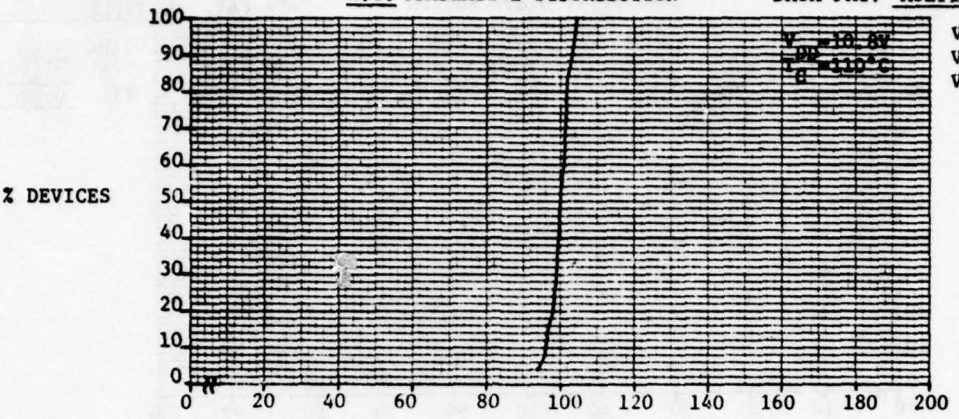
WRITE COMMAND HOLD TIME TO $\overline{RAS}$

t_{WCR}

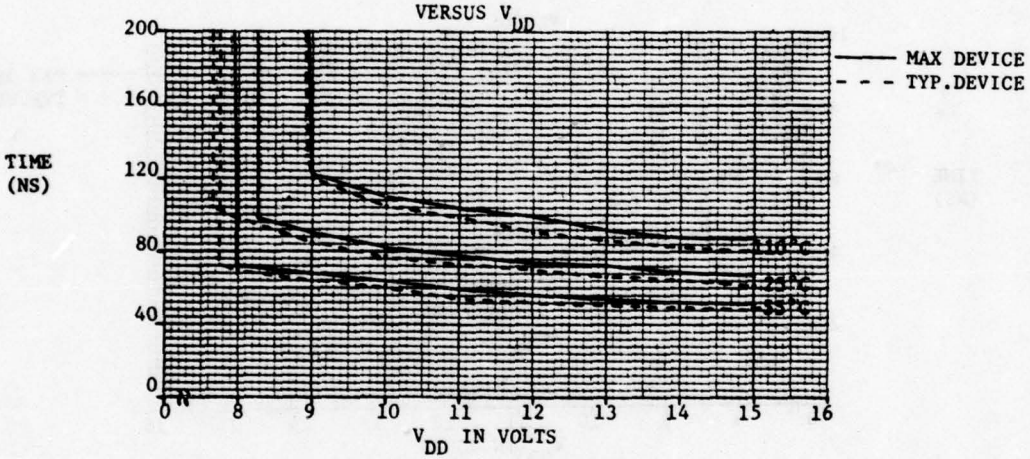
W.C. CUMULATIVE DISTRIBUTION

By J.F.& F.N. Date 1/27/78
V_{BB} -4.5V V_{CC} 5.0V
LOAD N.A.
ADDR PAT. MULTIPLE
DATA PAT. MULTIPLE

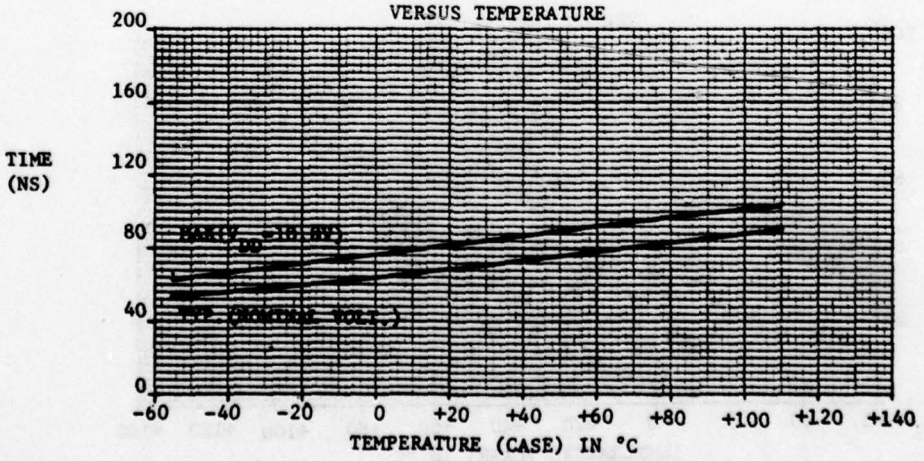
VIHC 2.7V
VIH 2.4V
VIL 0.8V



VERSUS V_{DD}



VERSUS TEMPERATURE



Vendor: A
P/N:
REV: G
Date Code: 7751
#DEVICES 25

16K DYNAMIC RAM

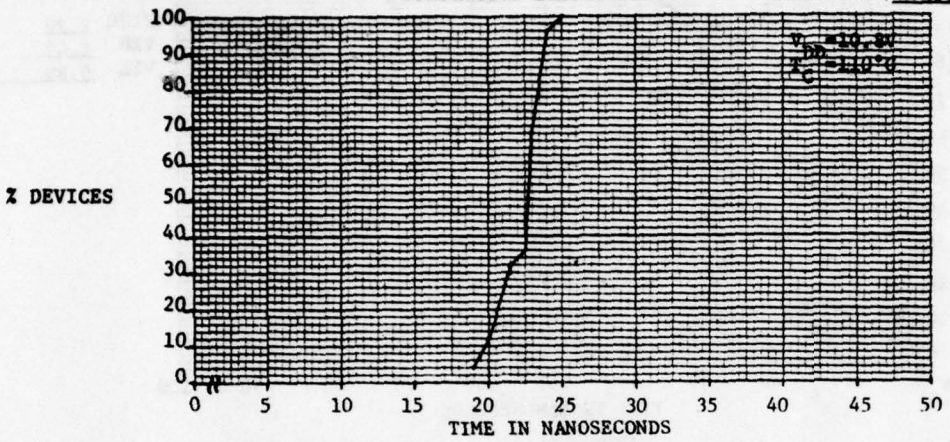
WRITE COMMAND PULSE WIDTH

t_{WP}

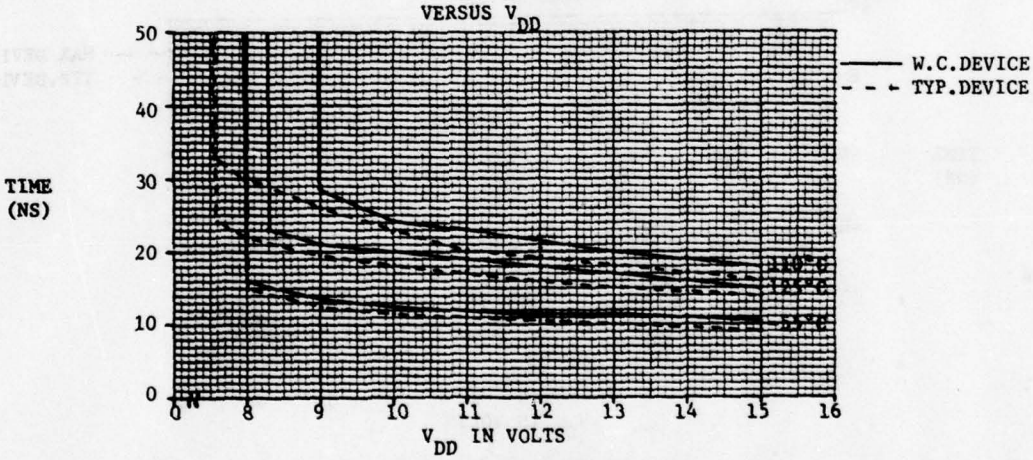
CUMULATIVE DISTRIBUTION

By F.N.& J.F. Date 2/1/78
V_{BB} -4.5V V_{CC} 5.0V
LOAD N.A.
ADDR PAT. MULTIPLE
DATA PAT. MULTIPLE

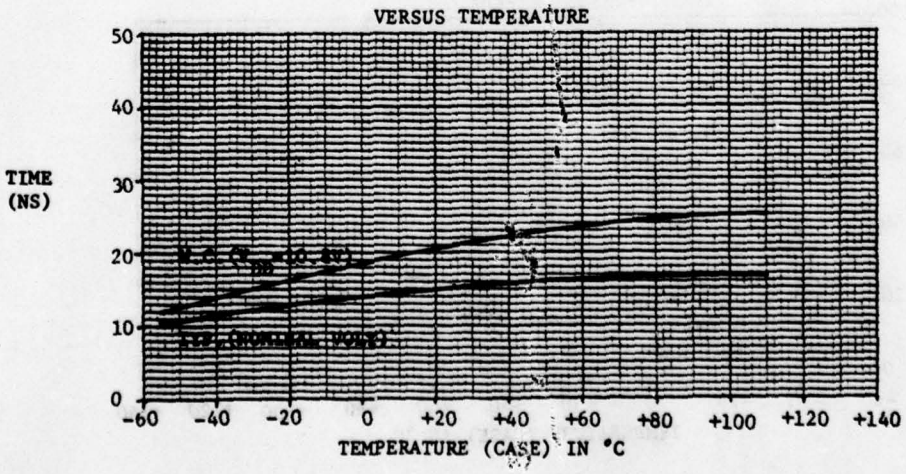
VIHC 2.7V
VIH 2.4V
VIL 0.8V



VERSUS V_{DD}



VERSUS TEMPERATURE



Vendor: A
P/N:
REV: G
Date Code: 7751
DEVICES 25

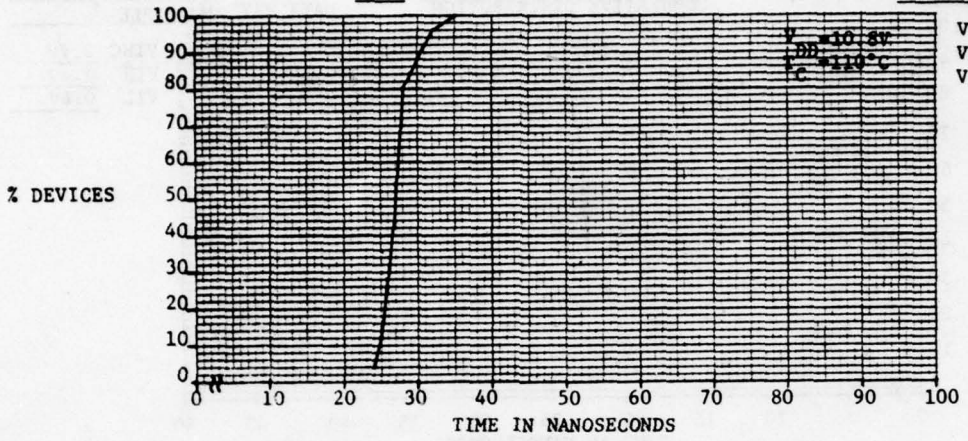
16K DYNAMIC RAM

WRITE COMMAND TO $\overline{RAS}$ LEAD TIME

t_{RWL}

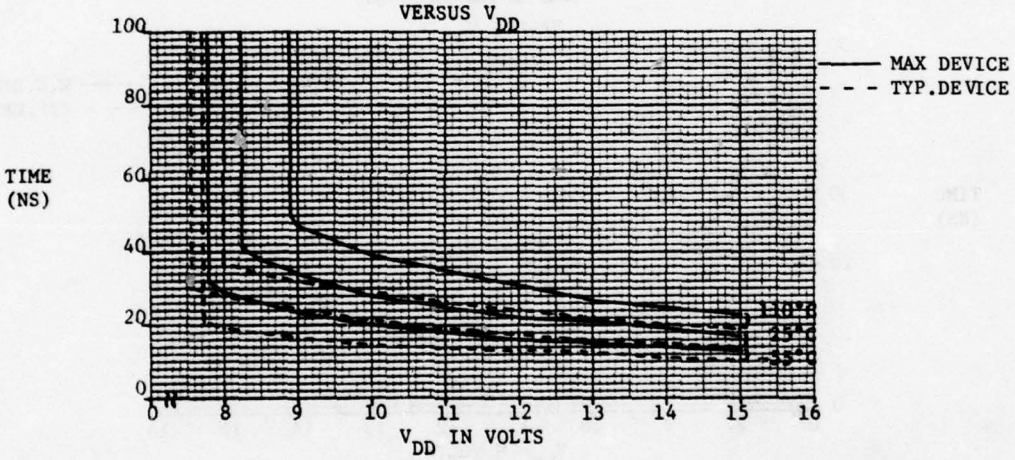
W.C. CUMULATIVE DISTRIBUTION

By J.F.& F.N. Date 1/26/78
V_{BB} -4.5V V_{CC} 5.0V
LOAD N.A.
ADDR PAT. MULTIPLE
DATA PAT. MULTIPLE

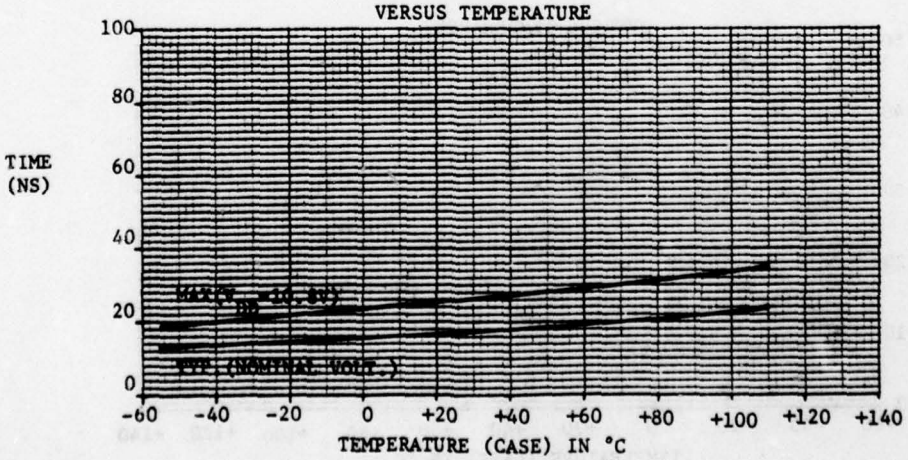


VIHC 2.7V
VIH 2.4V
VIL 0.8V

VERSUS V_{DD}



VERSUS TEMPERATURE

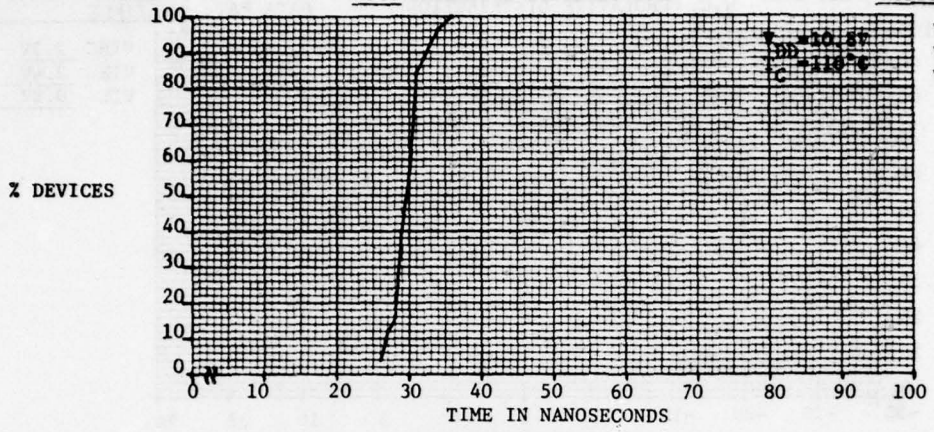


Vendor: A
P/N:
REV: G
Date Code: 7751
#DEVICES 25

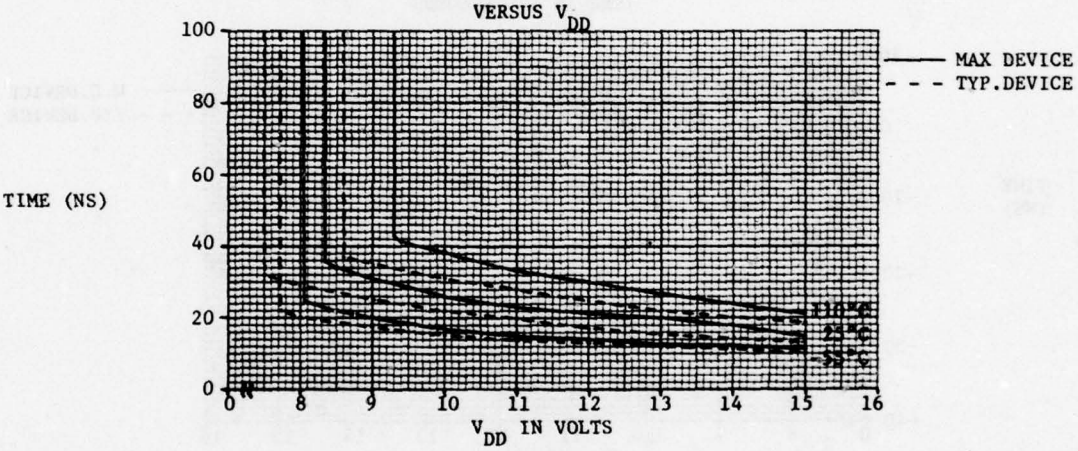
16K DYNAMIC RAM
WRITE COMMAND TO CAS LEAD TIME
t_{CWL}
W.C.CUMULATIVE DISTRIBUTION

By J.F.& F.N. Date 1/26/78
V_{BB} -4.5V V_{CC} 5.0V
LOAD N.A.
ADDR PAT. MULTIPLE
DATA PAT. MULTIPLE

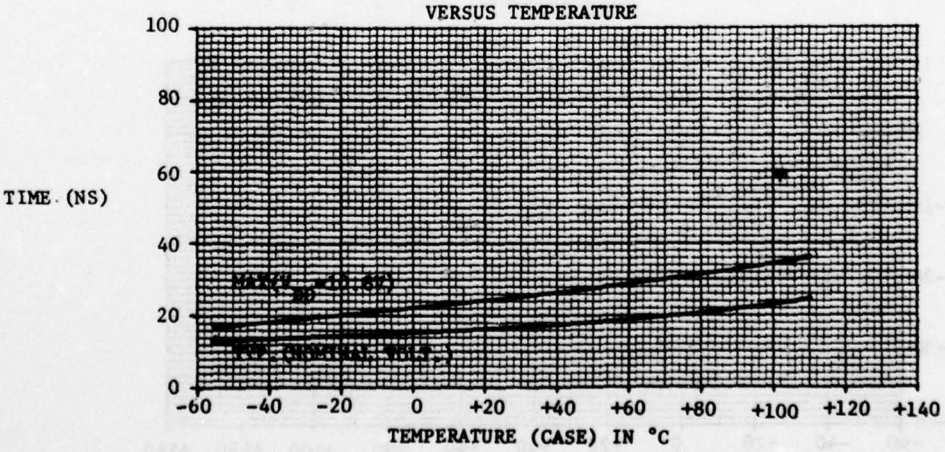
VIHC 2.7V
VIH 2.4V
VIL 0.8V



VERSUS V_{DD}



VERSUS TEMPERATURE



Vendor: A
P/N:
REV: G
Date Code: 7751
DEVICES 25

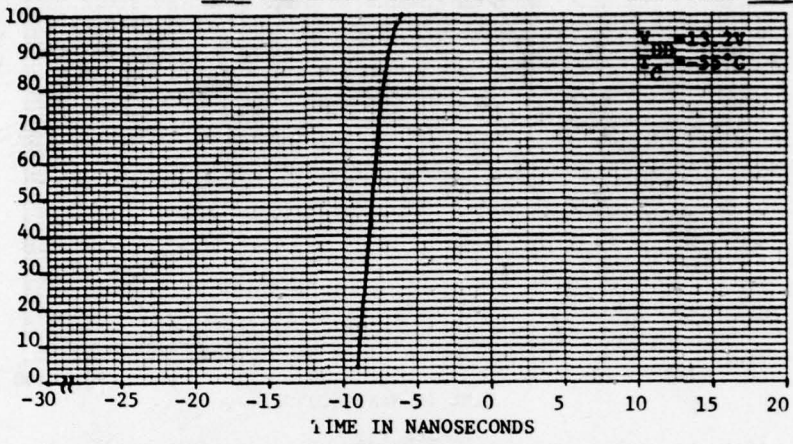
16K DYNAMIC RAM
DATA-IN SET-UP TIME
REFERENCED TO CAS

$t_{DS(C)}$

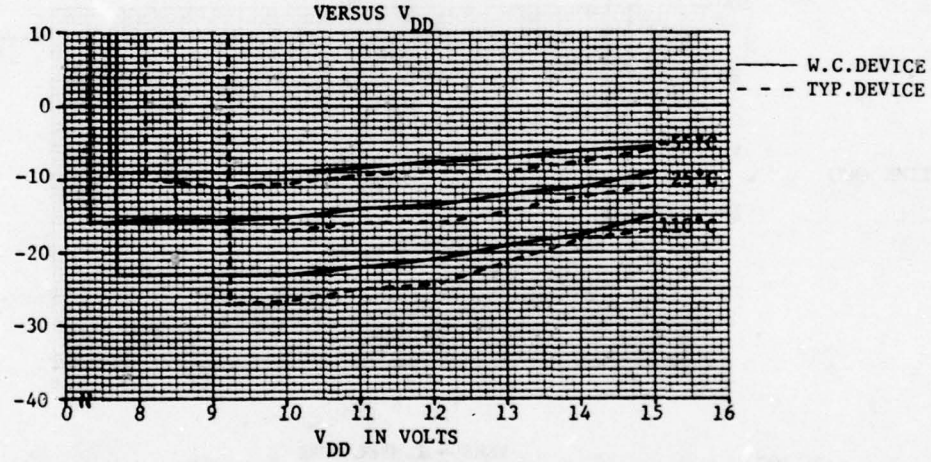
W.C. CUMULATIVE DISTRIBUTION

By J.F.& F.N. Date 2/3/78
V_{BB} -5.5V V_{CC} 5.0V
LOAD N.A.
ADDR PAT. MULTIPLE
DATA PAT. MULTIPLE

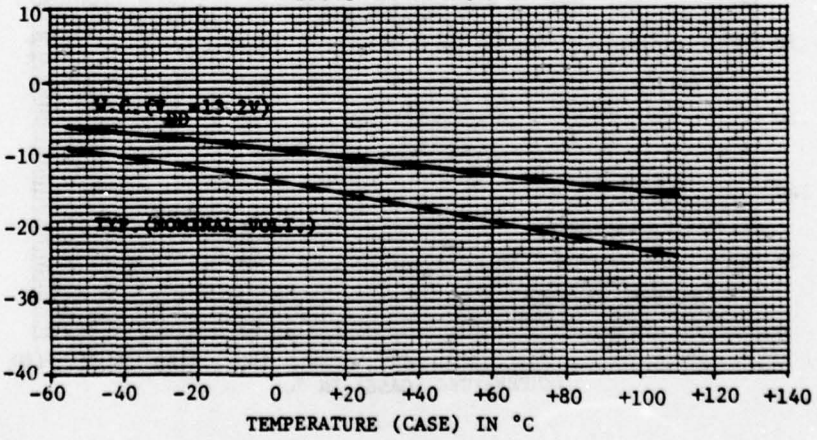
VIHC 2.7V
VIH 2.4V
VIL 0.8V



VERSUS V_{DD}



VERSUS TEMPERATURE

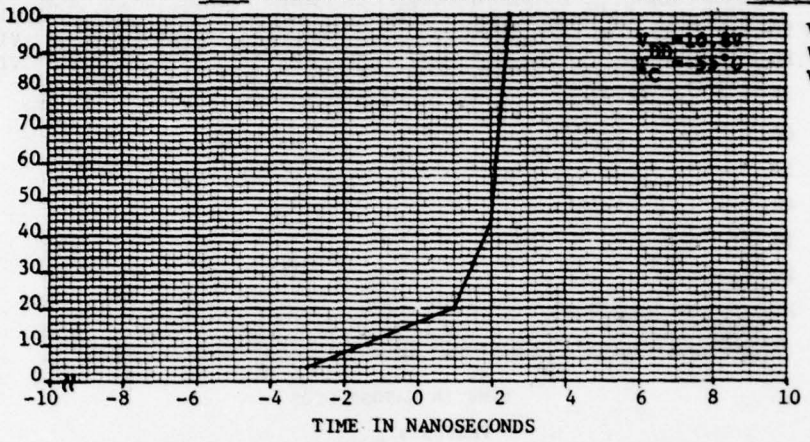


Vendor: A
P/N:
REV: G
Date Code: 7751
DEVICES 25

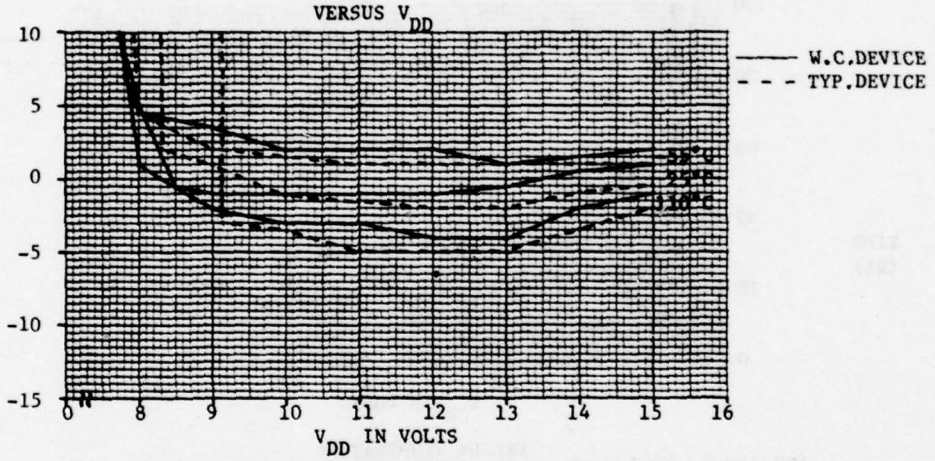
16K DYNAMIC RAM
DATA-IN SET-UP TIME
REFERENCED TO WRITE
$t_{DS(W)}$
W.C. CUMULATIVE DISTRIBUTION

By J.F.& F.N. Date 2/1/78
V_{BB} -4.5V V_{CC} 5.0V
LOAD N.A.
ADDR PAT. MULTIPLE
DATA PAT. MULTIPLE

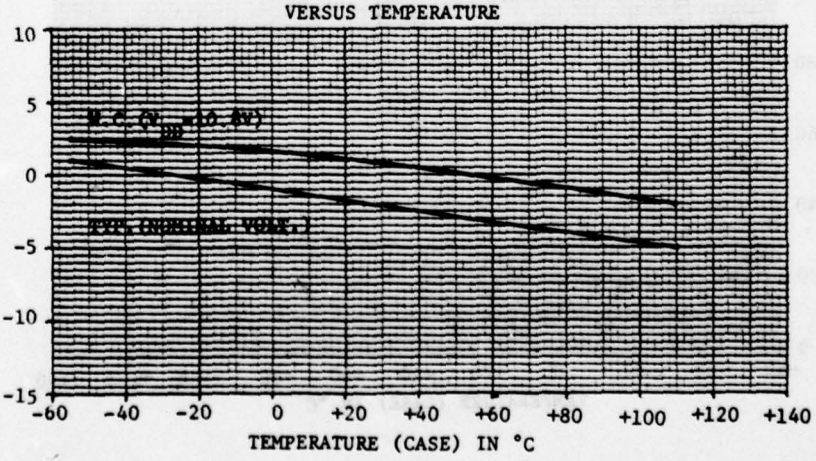
VIHC 2.7V
VIH 2.4V
VIL 0.8V



VERSUS V_{DD}



VERSUS TEMPERATURE



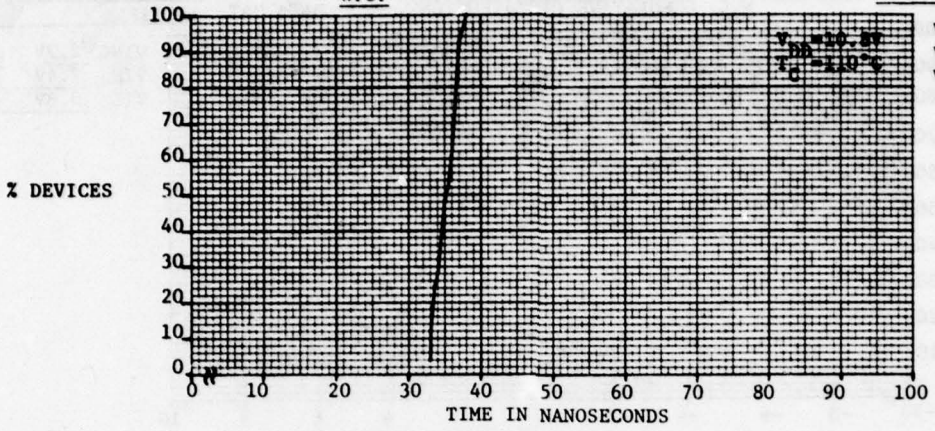
Vendor: A
P/N:
REV: G
Date Code: 7751
DEVICES 25

16K DYNAMIC RAM
DATA-IN HOLD TIME
REFERENCED TO CAS
$t_{DH(C)}$

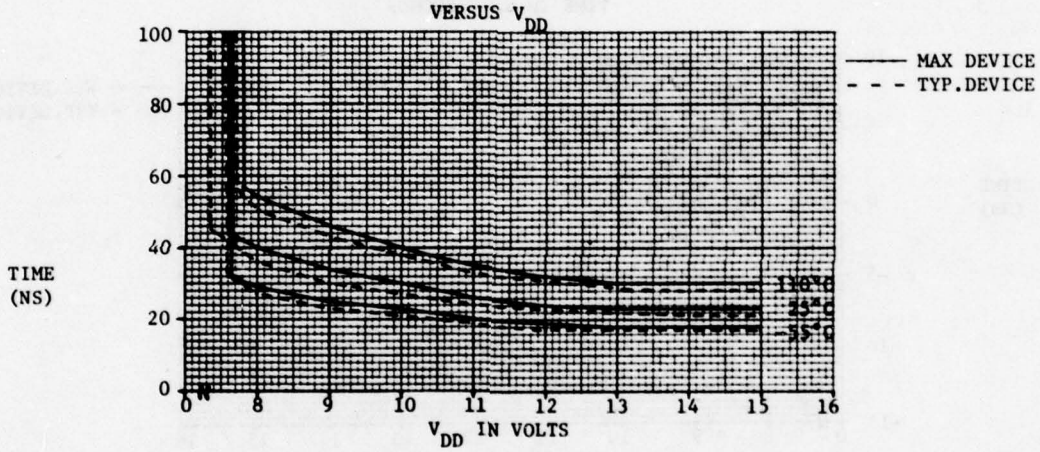
By J.F.& F.N. Date 2/2/78
V_{BB} -4.5V V_{CC} 5.0V
LOAD N.A.
ADDR PAT. MULTIPLE
DATA PAT. MULTIPLE

W.C. CUMULATIVE DISTRIBUTION

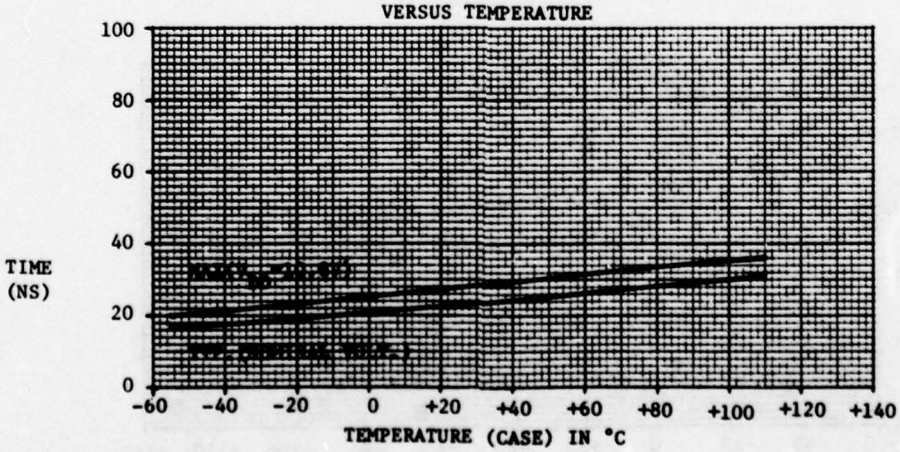
VIHC 2.7V
VIH 2.4V
VIL 0.8V



VERSUS V_{DD}



VERSUS TEMPERATURE



Vendor: A
P/N:
REV: G
Date Code: 7751
DEVICES 25

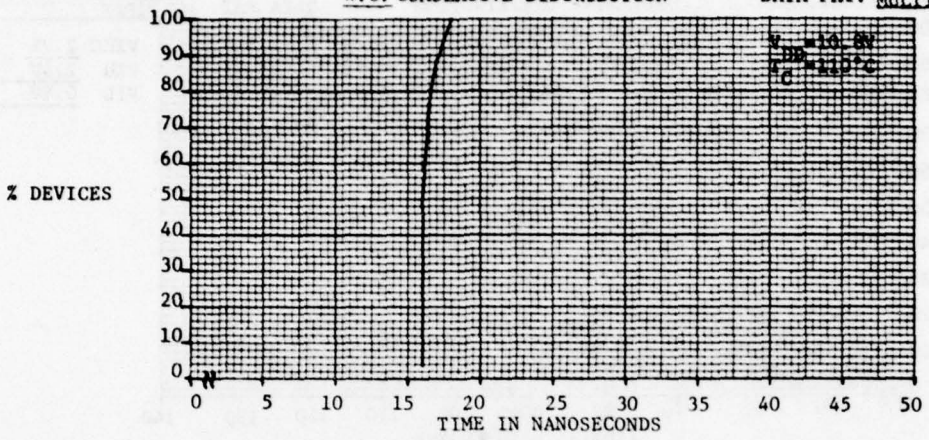
16K DYNAMIC RAM

DATA-IN HOLD TIME
REFERENCED TO WRITE
$t_{DH(W)}$

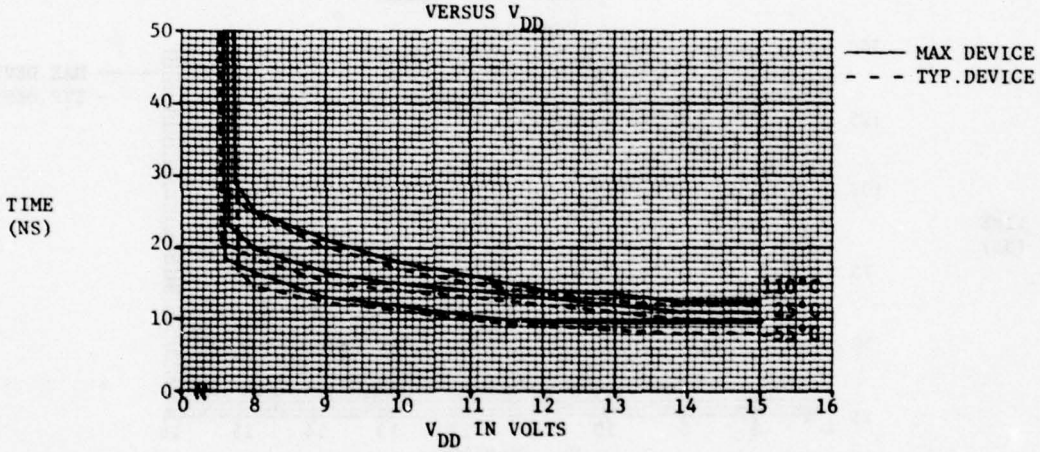
W.C. CUMULATIVE DISTRIBUTION

By J.F.& F.N. Date 2/2/78
V_{BB} -4.5V V_{CC} 5.0V
LOAD N.A.
ADDR PAT. MULTIPLE
DATA PAT. MULTIPLE

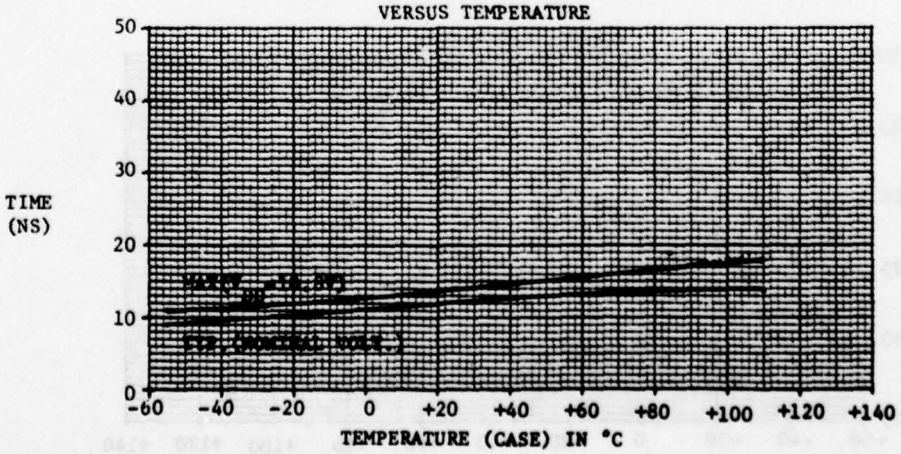
VIHC 2.7V
VIH 2.4V
VIL 0.8V



VERSUS V_{DD}



VERSUS TEMPERATURE

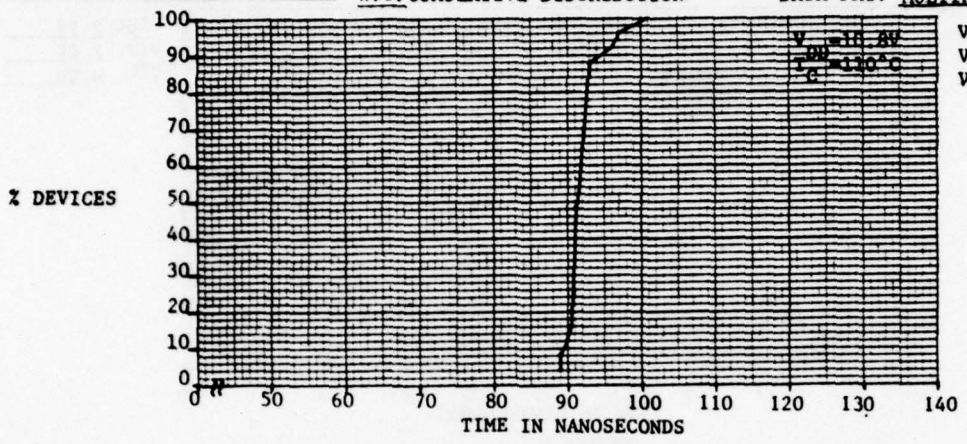


Vendor: A
P/N:
REV: G
Date Code: 7751
Devices: 25

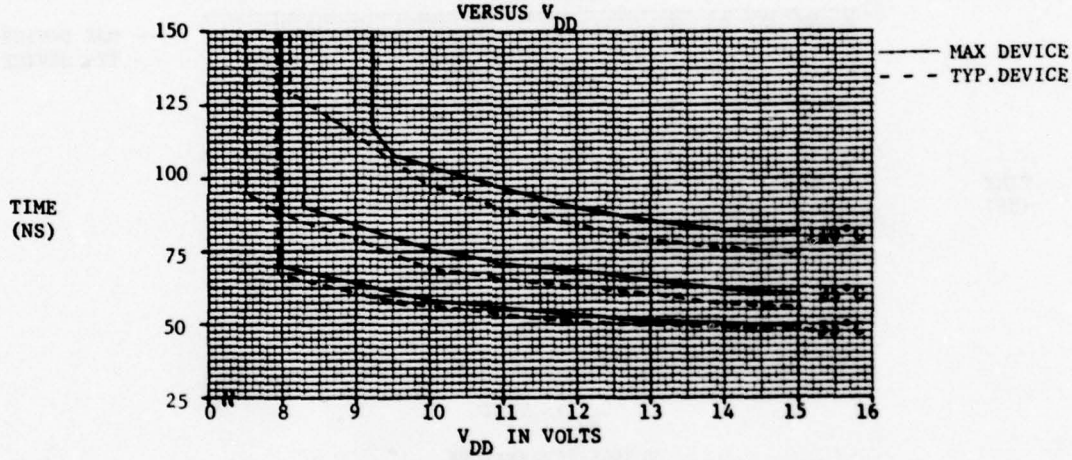
16K DYNAMIC RAM
DATA-IN HOLD TIME
REFERENCED TO $\overline{RAS}$
t_{DHR}
W.C. CUMULATIVE DISTRIBUTION

By J.F.&F.N. Date 2/1/78
V_{BB} -4.5V V_{CC} 5.0V
LOAD N.A.
ADDR PAT. MULTIPLE
DATA PAT. MULTIPLE

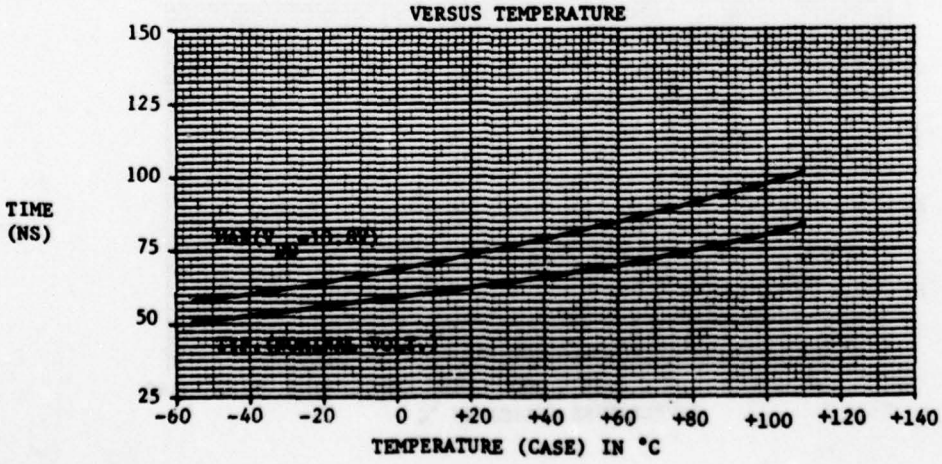
VIHC 2.7V
VIH 2.4V
VIL 0.8V



VERSUS V_{DD}



VERSUS TEMPERATURE

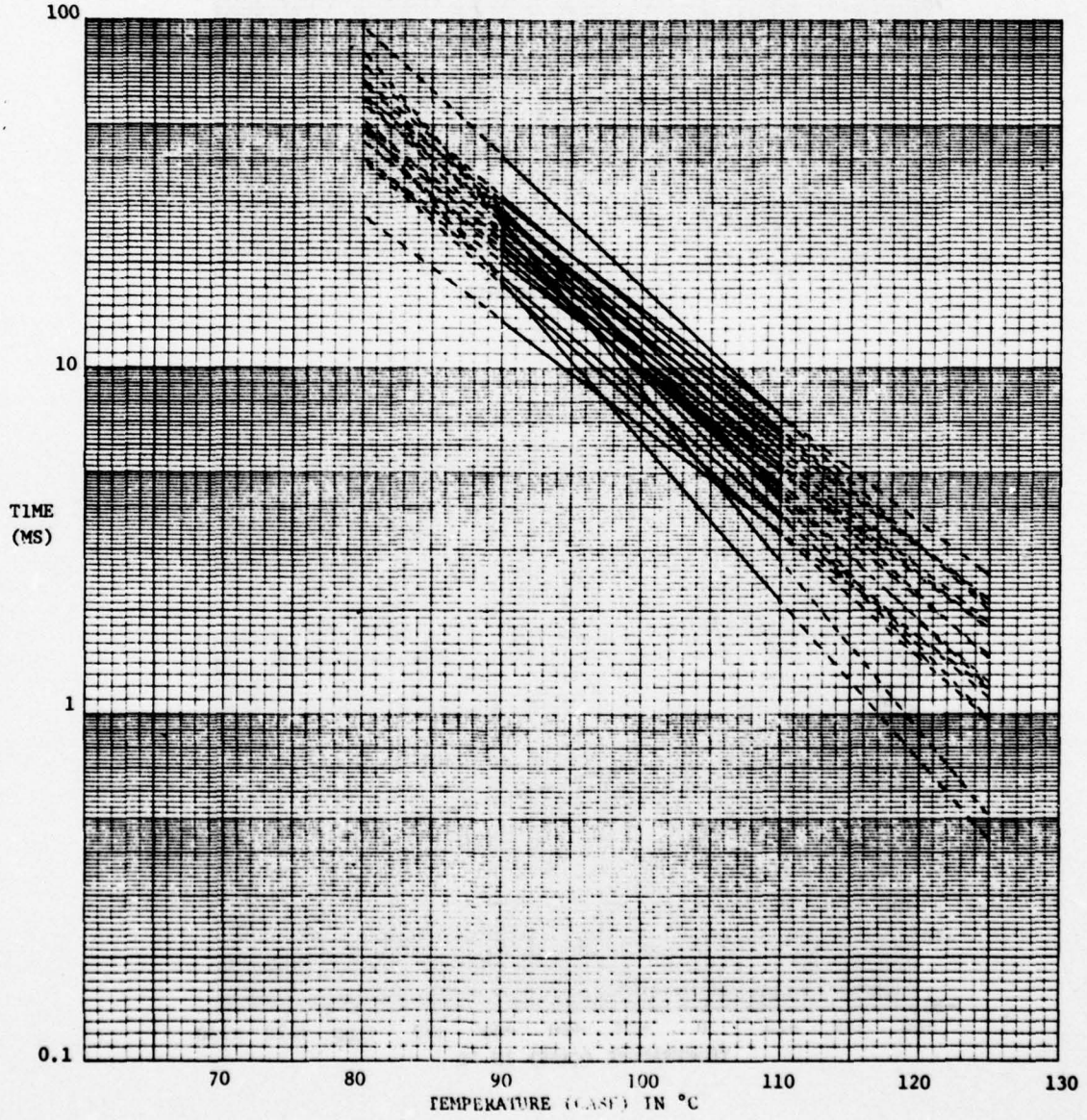


16K DYNAMIC RAM

Vendor: A
P/N:
REV: G
Date Code: 7751
devices 25

CELL RETENTION TIME
REFRESH PERIOD t_{REF}

By J.R.F. Date 1/12/78
V_{DD} 10.8V V_{BB} -5.0V
ADDR. PAT. DYNAMIC REFRESH
DATA PAT. SINGLE X-BAR
V_{IHC} 2.7V
V_{IH} 2.4V
V_{IL} 0.8V

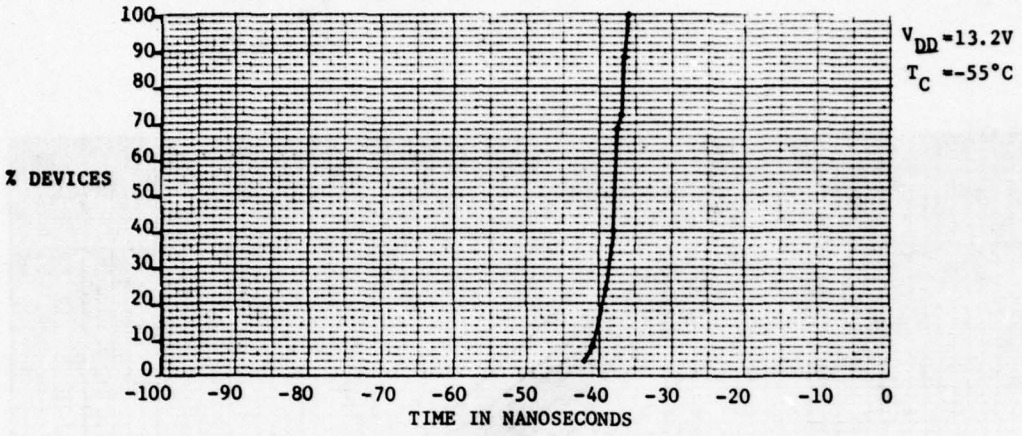


Vendor: A
P/N:
REV: G
Date Code: 7751
DEVICES 25

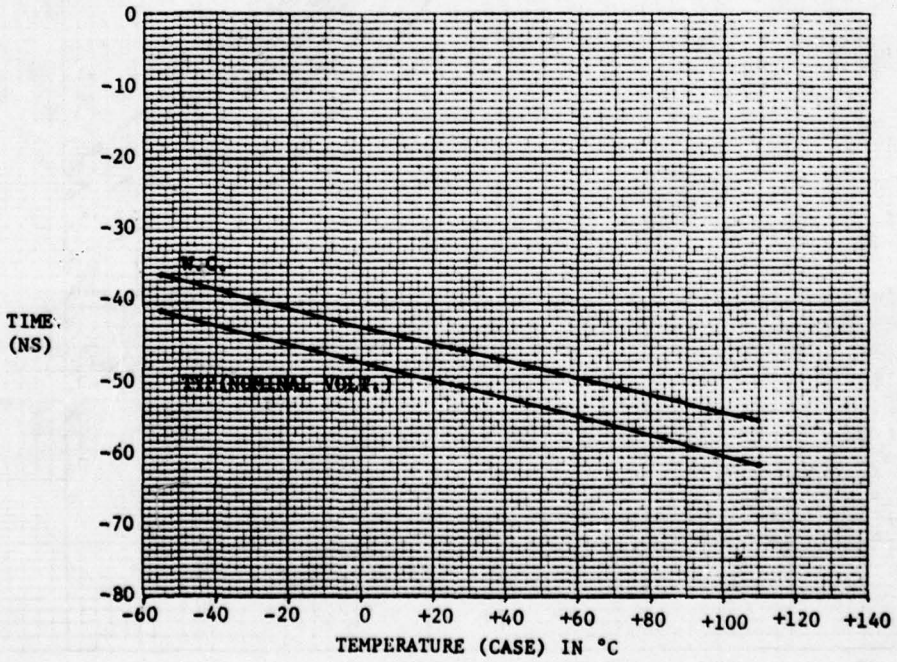
16K DYNAMIC RAM
WRITE COMMAND SET-UP TIME
t_{WCS}

By J.F.& F.N. Date 2/11/78
V_{BB} -5.5V V_{CC} 5.0V
LOAD N.A.
ADDR PAT. MULTIPLE
DATA PAT. MULTIPLE

W.C. CUMULATIVE DISTRIBUTION



VERSUS TEMPERATURE



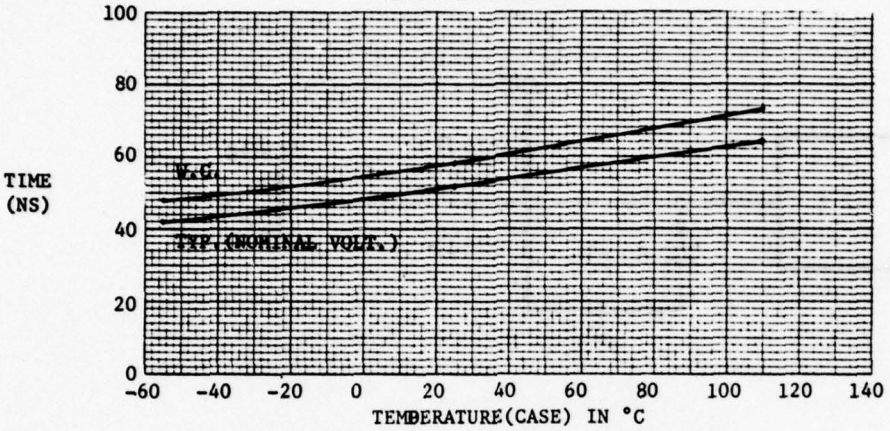
Vendor: A
P/N:
REV.: G
Date Code: 7751
DEVICES: 25

16K DYNAMIC RAM

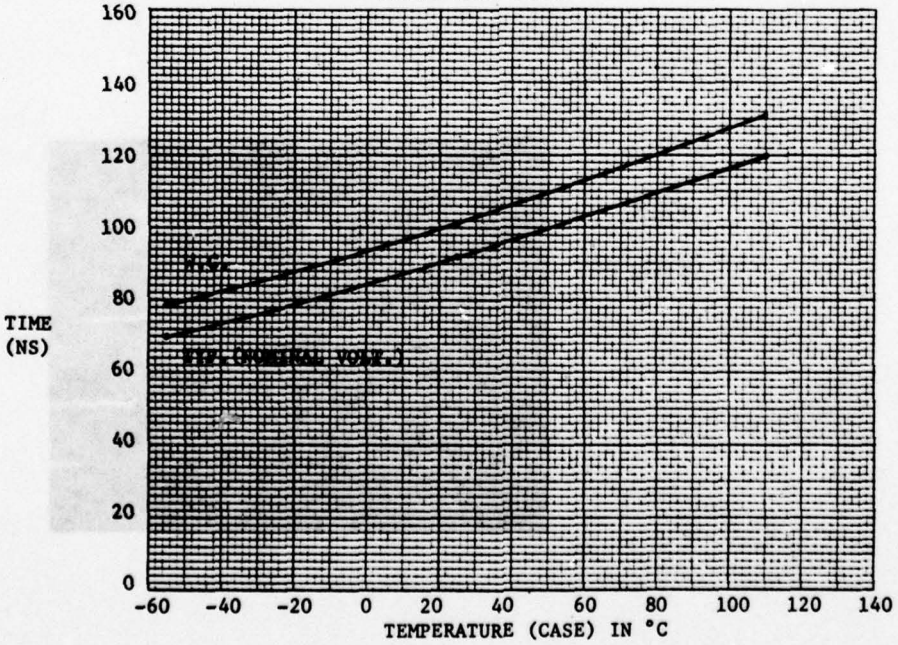
By: J.F.& F.N. Date 2/10/78
LOAD N.A.
ADDR.PAT. MULTIPLE
DATA PAT. MULTIPLE

V_{DD} = 10.8V
V_{BB} = -4.5V
V_{CC} = 5.0V

$\overline{CAS}$ TO WRITE DELAY (t_{CWD})
VERSUS TEMPERATURE



$\overline{RAS}$ TO WRITE DELAY (t_{RWD})
VERSUS TEMPERATURE

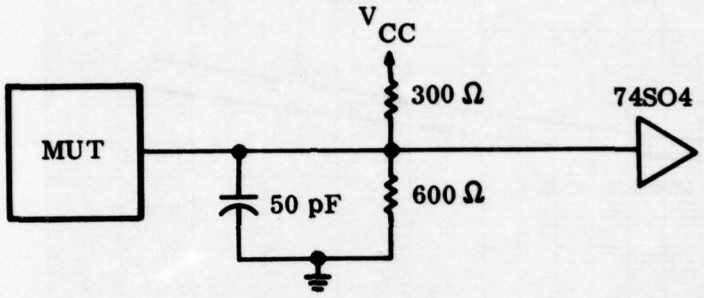


Output Turn-Off Delay

$\overline{CAS}$ Rise to Output High-Z

Measurement reference levels:

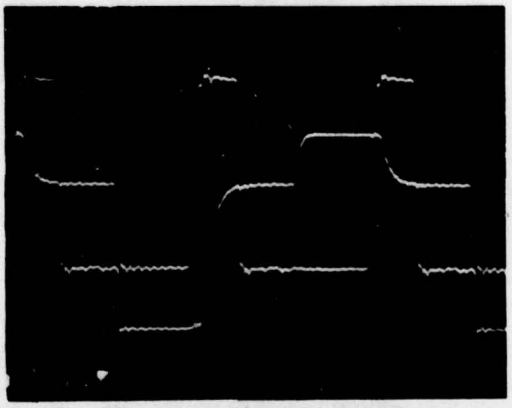
1.5 V to 10% change on output



Load Configuration

$\overline{CAS}$

Data out



Unexpanded View, Depicting Data Out with Respect to $\overline{CAS}$

Output Turn-Off Delay

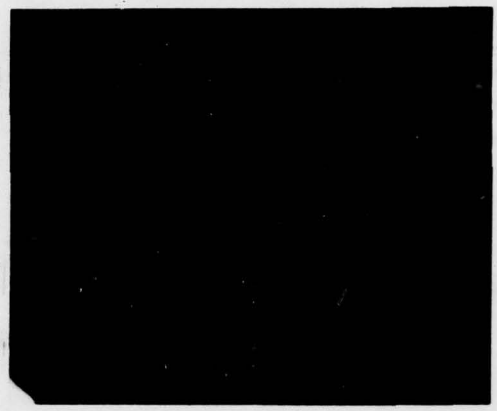
$\overline{CAS}$ Rise to Output High-Z

Measured:

1.5 V to 10% change on output

W.C.P.S.
V_{DD}=13.2 V
V_{BB}=-5.5 V
V_{CC}= 5.0 V

110°C(case)
t_{OFF}=28 ns

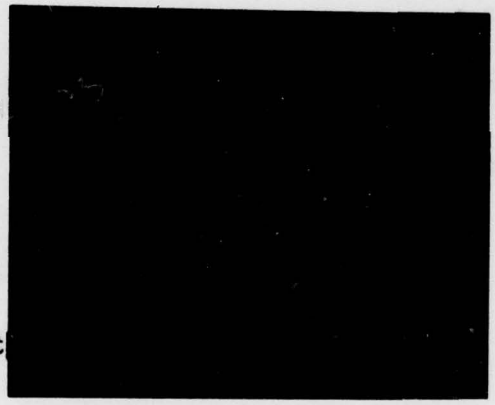


VENDOR A

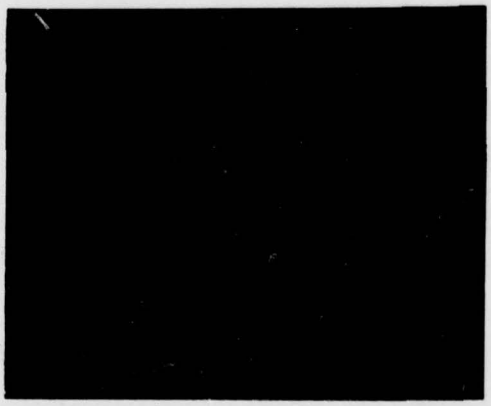
Rev G
D.C. 7751

Maximum unit 10

25°C(case)
t_{OFF}=24 ns



-55°C(case)
t_{OFF}=19 ns



Output Turn-Off Delay

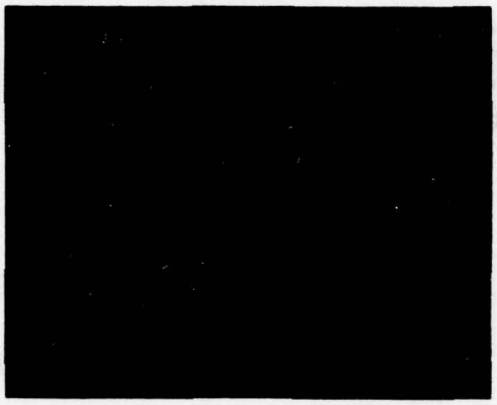
$\overline{CAS}$ Rise to Output High-Z

Measured:

1.5 V to 10% change on output

W.C.P.S.
V_{DD}=13.2 V
V_{BB}=-5.5 V
V_{CC}= 5.0 V

110°C(case)
t_{OFF}=25 ns



VENDOR A

Rev G
D.C. 7751

Minimum unit 24

25°C(case)
t_{OFF}=21 ns

-55°C(case)
t_{OFF}=16 ns

Output Turn-Off Delay

$\overline{\text{CAS}}$ Rise to Output High-Z

Measured:

1.5 V to 10% change on output

W.C.P.S.
V_{DD}=13.2 V
V_{BB}=-5.5 V
V_{CC}= 5.0 V

110°C(case)
t_{OFF}=27 ns

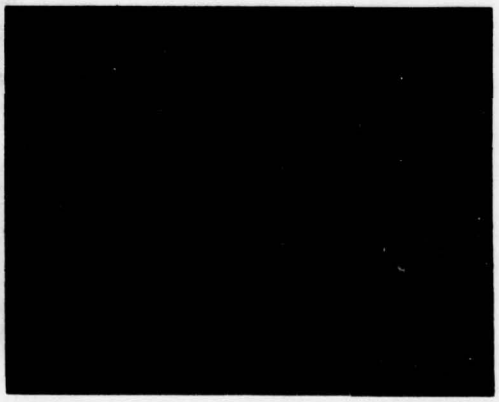
VENDOR A

Rev G
D.C. 7751

Typical Unit 14

25°C(case)
t_{OFF}=23 ns

-55°C(case)
t_{OFF}=19 ns



Output Turn-Off Delay

$\overline{CAS}$ Rise to Output High-Z

Measured:

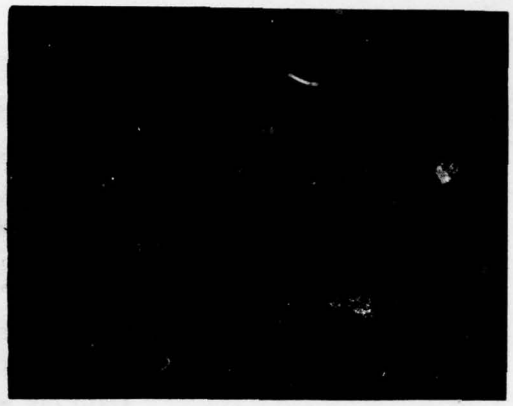
1.5 V to 10% change on output

W.C.P.S.
V_{DD}=13.2 V
V_{BB}=-5.5 V
V_{CC}= 5.0 V

Data Out

110°C(case)
t_{OFF}=30 ns

$\overline{CAS}$



VENDOR A

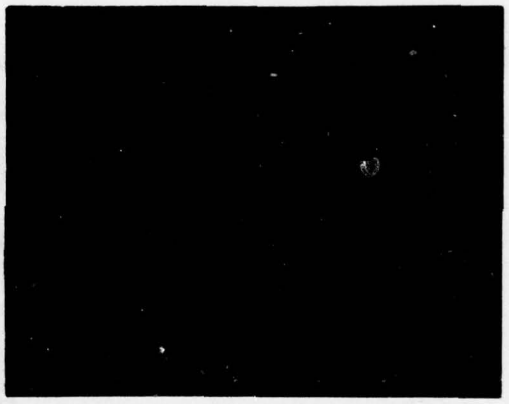
Rev G
D.C. 7751

Maximum unit 10

Data out

25°C(case)
t_{OFF}=25 ns

$\overline{CAS}$



Data out

-55°C(case)
t_{OFF}=22 ns

$\overline{CAS}$

Output Turn-Off Delay

$\overline{CAS}$ Rise to Output High-Z

Measured:

1.5 V to 10% change on output

W.C.P.S.
V_{DD}=13.2 V
V_{BB}=-5.5 V
V_{CC}= 5.0 V

Data out

110°C(case)
t_{OFF}=28 ns

$\overline{CAS}$

VENDOR A

Rev G
D.C. 7751

Typical unit 14

Data out

25°C(case)
t_{OFF}=25 ns

$\overline{CAS}$

Data out

-55°C(case)
t_{OFF}=21 ns

$\overline{CAS}$

Output Turn-Off Delay

$\overline{\text{CAS}}$ Rise to Output High-Z

Measured:

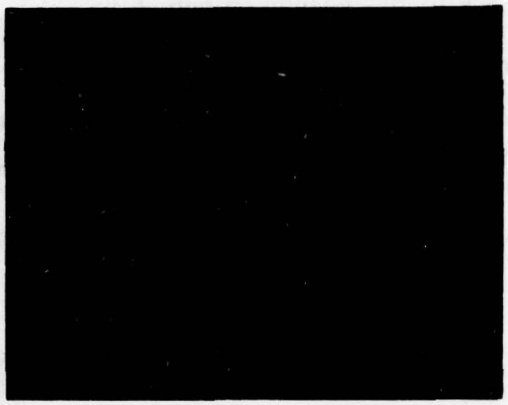
1.5 V to 10% change on output

W.C.P.S.
V_{DD}=13.2 V
V_{BB}=-5.5 V
V_{CC}= 5.0 V

Data out

110°C(case)
t_{OFF}=26 ns

$\overline{\text{CAS}}$



VENDOR A

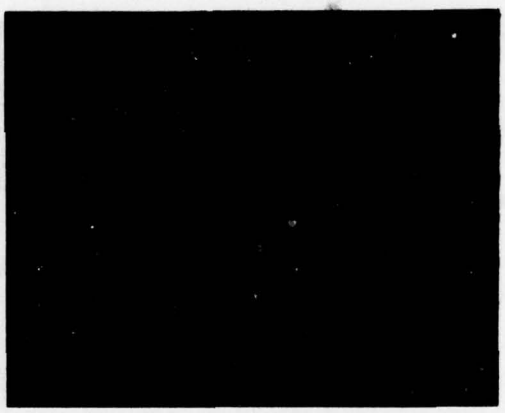
Rev G
D.C. 7751

Minimum unit 24

Data out

25°C(case)
t_{OFF}=23 ns

$\overline{\text{CAS}}$



Data out

-55°C(case)
t_{OFF}=18 ns

$\overline{\text{CAS}}$

16K DYNAMIC RAM

DEVICE CAPACITANCE

VENDOR A

REV.G
D.C. 7751

Device input and output capacitance measurements were made using a BOONTON Model 75B-S8 capacitance bridge. This bridge uses a test frequency of 1.0 MHZ. The test signal amplitude was set at 20MV P-P.

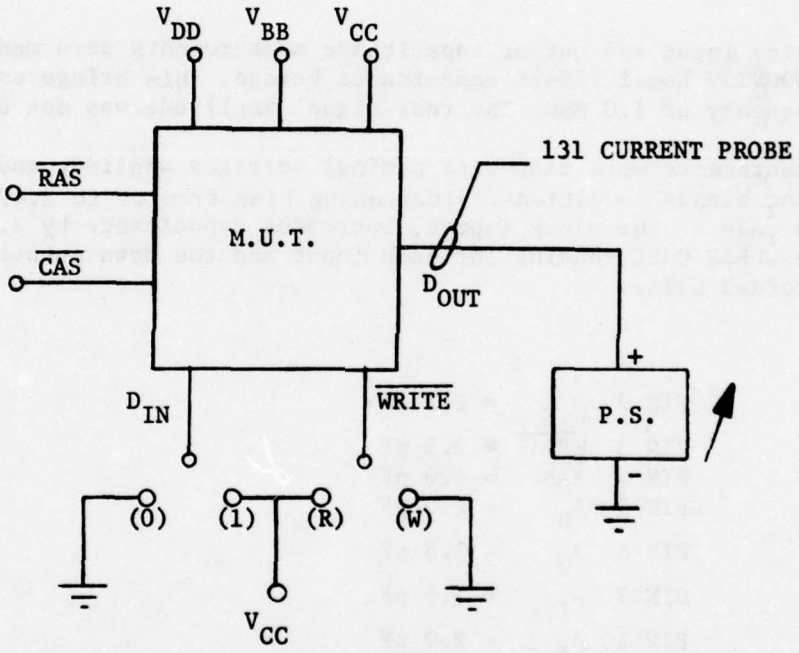
Measurements were made with nominal voltages applied, and taken under biased conditions. Increasing bias from 0V to 2.4V or 2.7V in the case of the clock inputs, increases capacitance by 1.0 to 1.5 pF. The WORSE CASE reading for each input and the data output pin are recorded below.

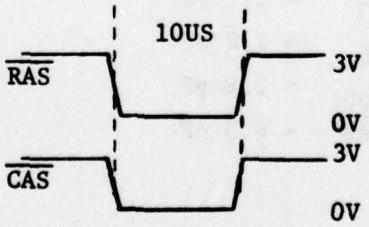
PIN 2	D_{IN}	= 2.1 pF
PIN 3	$\overline{WRITE}$	= 3.5 pF
PIN 4	$\overline{RAS}$	= 4.0 pF
PIN 5	A_0	= 2.0 pF
PIN 6	A_2	= 1.8 pF
PIN 7	A_1	= 1.9 pF
PIN 10	A_5	= 2.0 pF
PIN 11	A_4	= 1.9 pF
PIN 12	A_3	= 2.1 pF
PIN 13	A_6	= 2.2 pF
PIN 14	D_{OUT}	= 2.8 pF
PIN 15	$\overline{CAS}$	= 4.3 pF

16K DYNAMIC RAM

DYNAMIC TEST SET-UP FOR OUTPUT CURRENT

SOURCE CURRENT (I_{OH})
SINK CURRENT (I_{OL})





16K DYNAMIC RAM

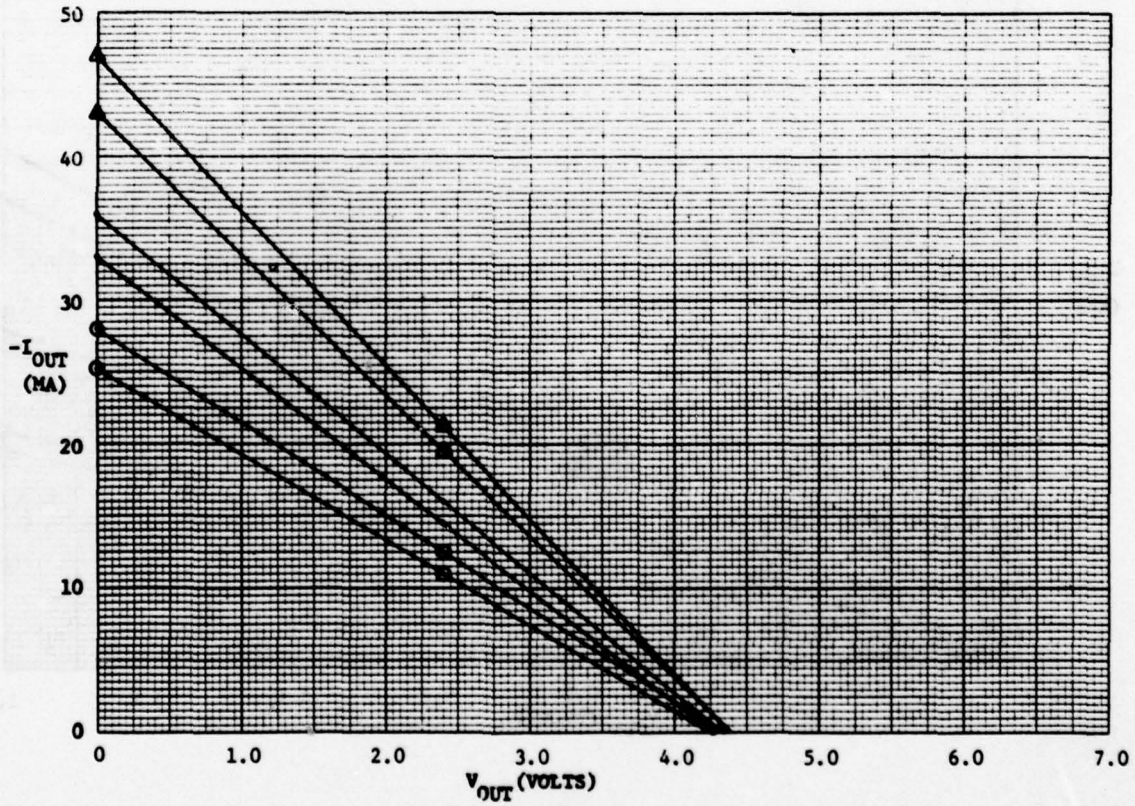
Vendor: A
P/N:
REV.: G
Date Code: 7751
DEV.: 23

SOURCE CURRENT(I_{OH})

By: F.A.N.
Date: 2/15/78

V_{DD} = 10.8V
V_{BB} = -5.5V
V_{CC} = 5.0V

• 25°C
⊙ 110°C
Δ -55°C



16K DYNAMIC RAM

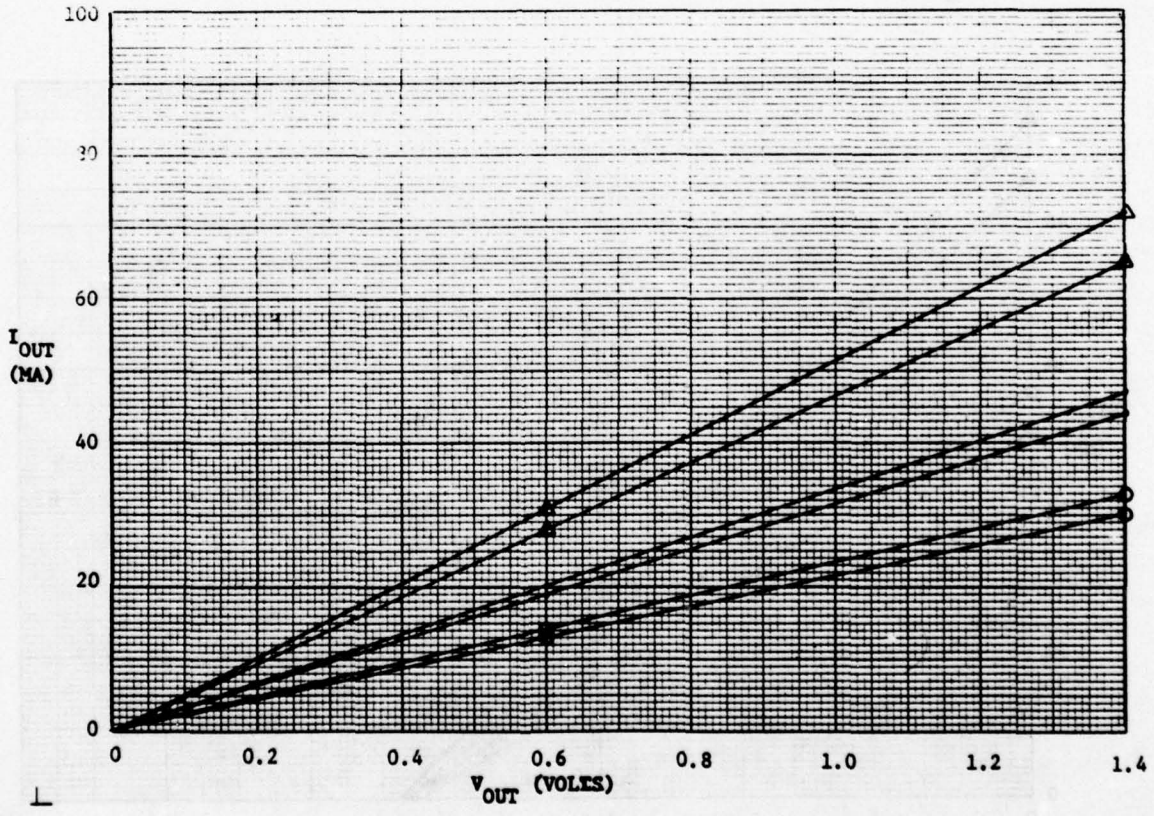
Vendor: A
P/N:
REV.: G
Date Code: 7751
DET.: 23

SINK CURRENT(I_{OL})

By: F.A.N.
Date: 2/15/78

V_{DD} = 10.8V
V_{BB} = -5.5V
V_{CC} = 5.0V

• 25°C
⊙ 110°C
△ -55°C



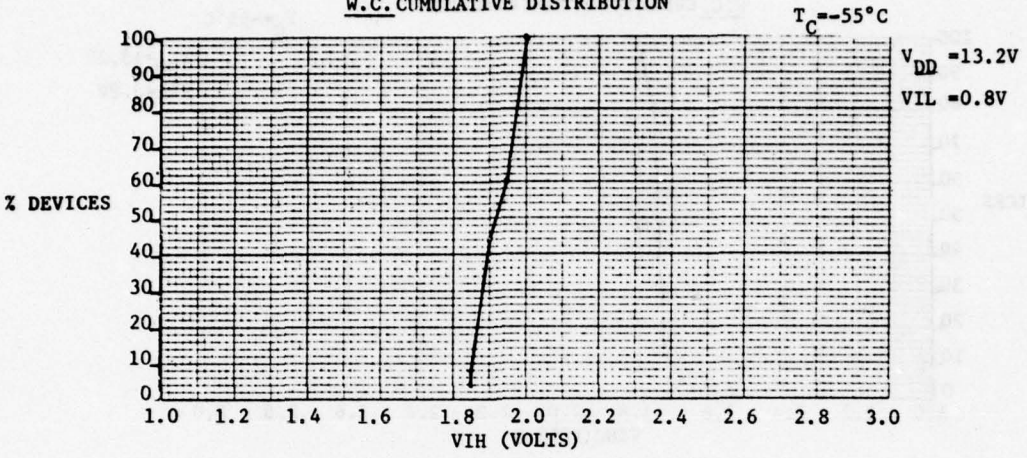
IBM

Vendor: A
P/N:
REV: G
Date Code: 7751
DEVICES 25

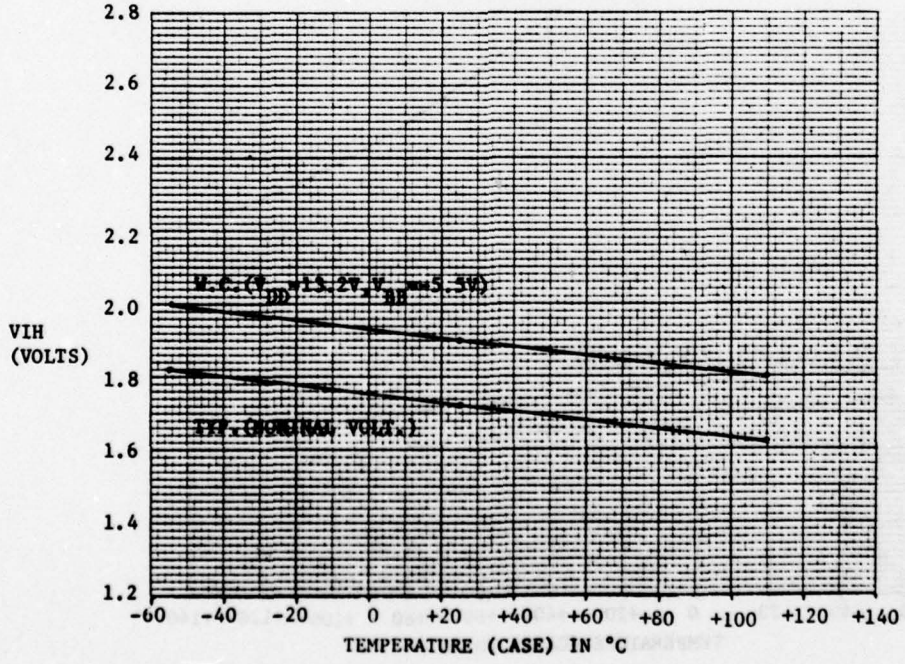
16K DYNAMIC RAM
MINIMUM INPUT UP LEVEL
(ANY INPUT)
VIH

By J.F.& F.N. Date 2/9/78
V_{BB} -5.5V V_{CC} 5.0V
LOAD N.A.
ADDR PAT. MULTIPLE
DATA PAT. MULTIPLE

DATA BASED ON ADDR. INP. (W.C.)
W.C. CUMULATIVE DISTRIBUTION



VERSUS TEMPERATURE



IBM

Vendor: A
P/N:
REV: G
Date Code: 7751
DEVICES 25

16K DYNAMIC RAM

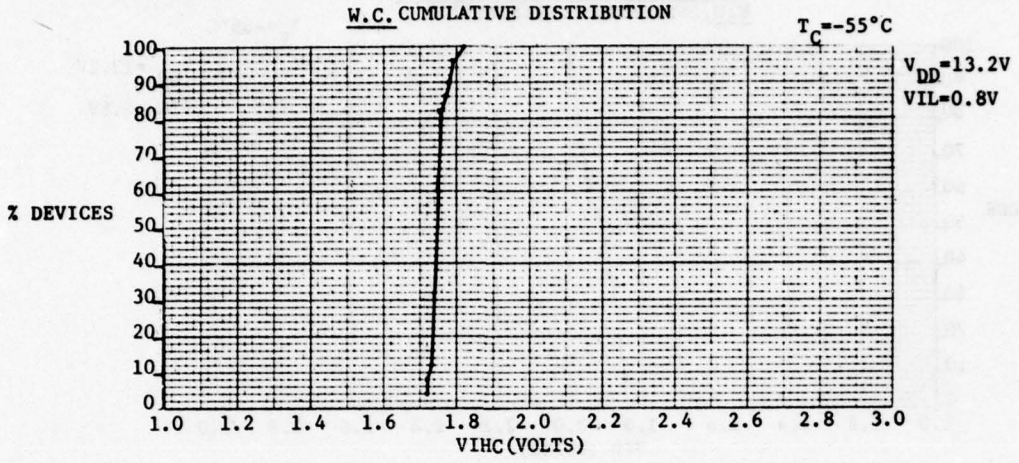
MINIMUM CLOCK INPUT UP LEVEL
(ANY CLOCK)

VIHC

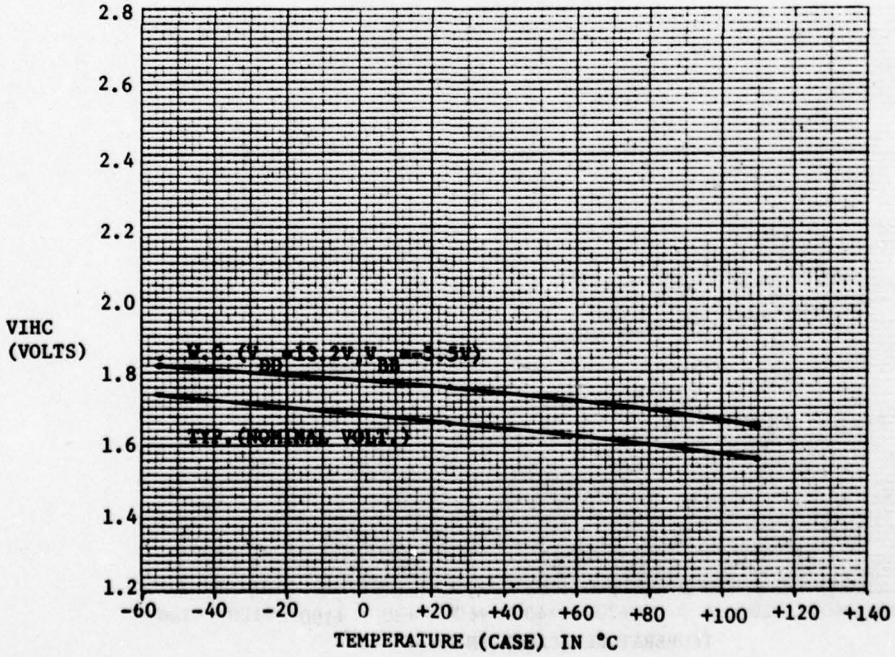
DATA BASED ON $\overline{RAS}$ INPUT (W.C.)

By J.F.& F.N. Date 1/9/78
V_{BB} -5.5V V_{CC} 5.0V
LOAD N.A.
ADDR PAT. MULTIPLE
DATA PAT. MULTIPLE

W.C. CUMULATIVE DISTRIBUTION



VERSUS TEMPERATURE

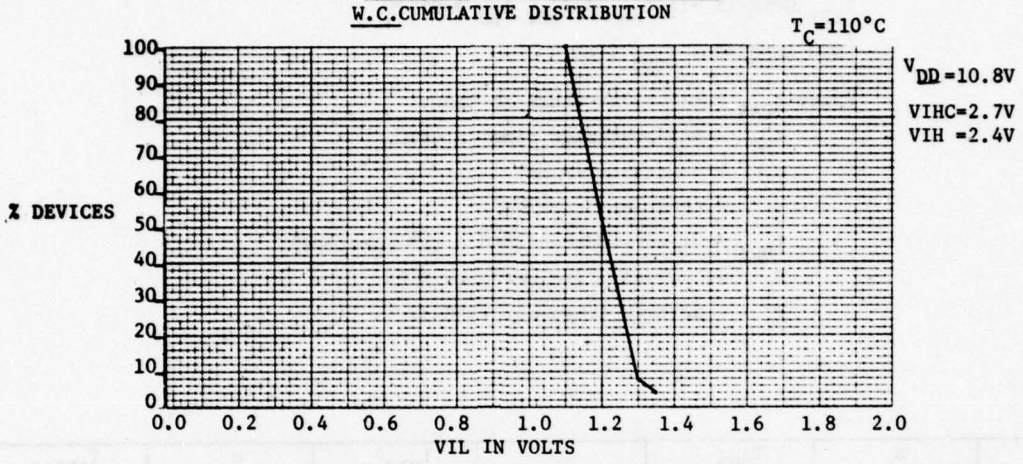


Vendor: A
P/N:
REV: G
Date Code: 7751
DEVICES 25

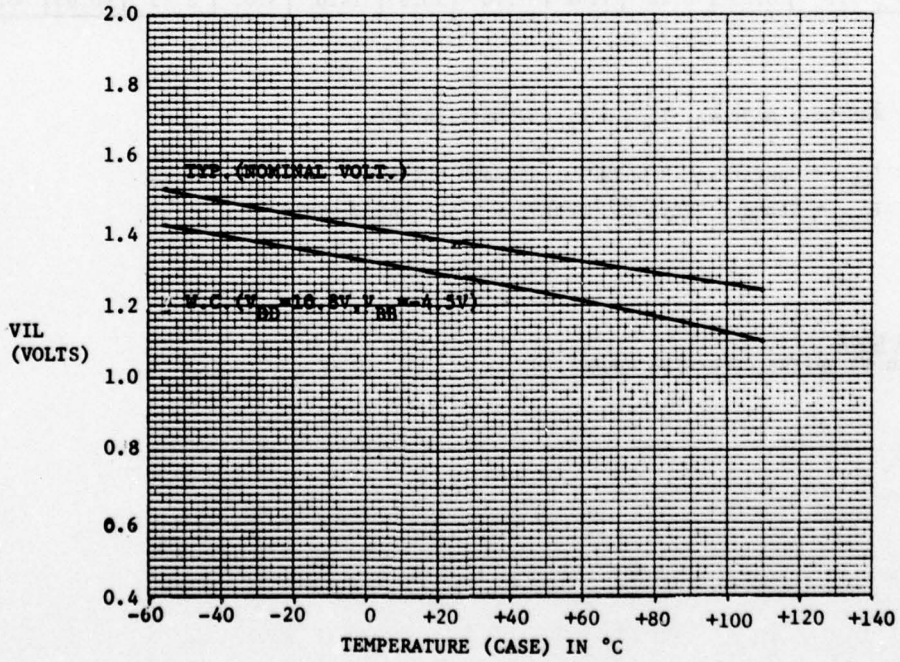
16K DYNAMIC RAM
MAXIMUM INPUT DOWN LEVEL
(ANY INPUT)
VIL

By J.F.& F.N. Date 2/8/78
V_{BB} -4.5V V_{CC} 5.0V
LOAD N.A.
ADDR PAT. MULTIPLE
DATA PAT. MULTIPLE

DATA BASED ON $\overline{RAS}$ INPUT (W.C.)
W.C.CUMULATIVE DISTRIBUTION



VERSUS TEMPERATURE



POWER CALCULATION CHART

I_{DD1} OPERATE $= (a\ t_{RAS} + I_{DD2}\ t_{RP} + b)\ F_1$

I_{DD3} REFRESH $= I_{DD2} + cF_2$

Where t_{RAS} = $\overline{RAS}$ pulse width in USEC.

t_{RP} = $\overline{RAS}$ precharge time in USEC.

a,b = constants in MA.

c = constant in MA/MHZ.

I_{DD2} = Standby Current($\overline{RAS}$ & $\overline{CAS}$ inactive)

F_1 = Operating frequency in MHZ.

F_2 = Refresh frequency in MHZ.

	a		I_{DD2}		b		I_{DD3}*		c		$I_{BB1\&3}$	
TEMP.	TYP.	MAX	TYP.	MAX	TYP.	MAX	TYP.	MAX	TYP.	MAX	TYP.	MAX
-55°C	5.20	6.0	0.47	0.54	7.47	7.95	15.3	15.8	5.57	5.72	-0.10	-0.13
+25°C	3.24	3.8	0.33	0.54	7.47	7.67	14.3	14.7	5.23	5.36	-0.05	-0.06
+110°C	2.02	2.3	0.23	0.28	7.42	7.70	13.6	14.0	5.02	5.15	-0.03	-0.035

* $\overline{RAS}$-Only Refresh, I_{DD3} @ t_{RC}=375NS(2.667MHZ.)

I_{BB1} = Operating (2.667MHZ.) SUBRATE CURRENT.

I_{BB2} = Standby SUBTRATE CURRENT = 1.5UA MAX @ -55°C

TEMPERATURE IS CASE
CURRENTS are in MA unless otherwise specified.

IBM

Vendor: A
P/N:
REV: G
Date Code: 7751
25 Units

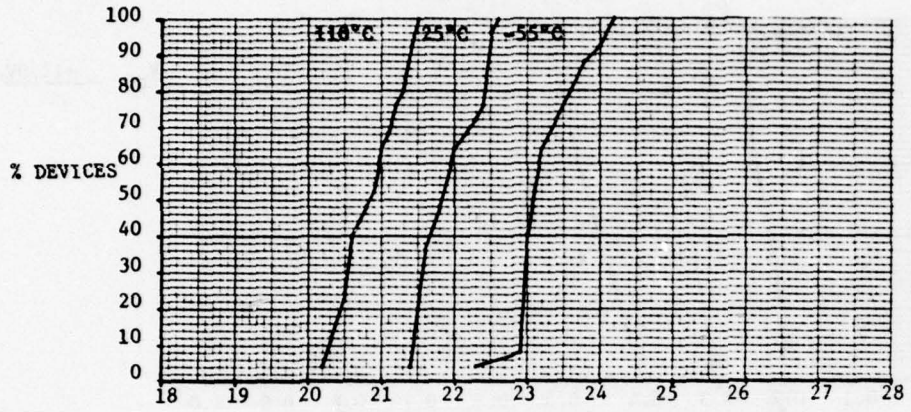
16K DYNAMIC RAM

OPERATING CURRENT

I_{DD1}

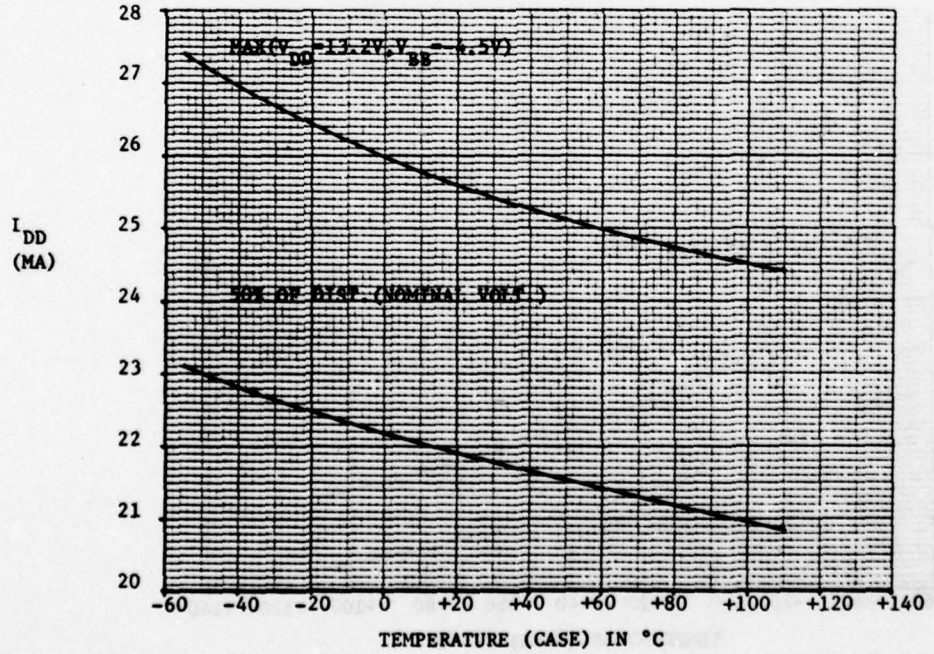
By J.R.F. Date 1/4/78
V_{BB} -5.0V V_{CC} +5.0V
LOAD 1 SCHOTTKY TTL + 50 pFd
ADDR PAT. WALKING DIAGONAL
DATA PAT. MAJOR DIAGONAL

CUMULATIVE DISTRIBUTION



V_{DD} +12.0V
t_{RC} 375 NS
t_{RAS} 250 NS

VERSUS TEMPERATURE



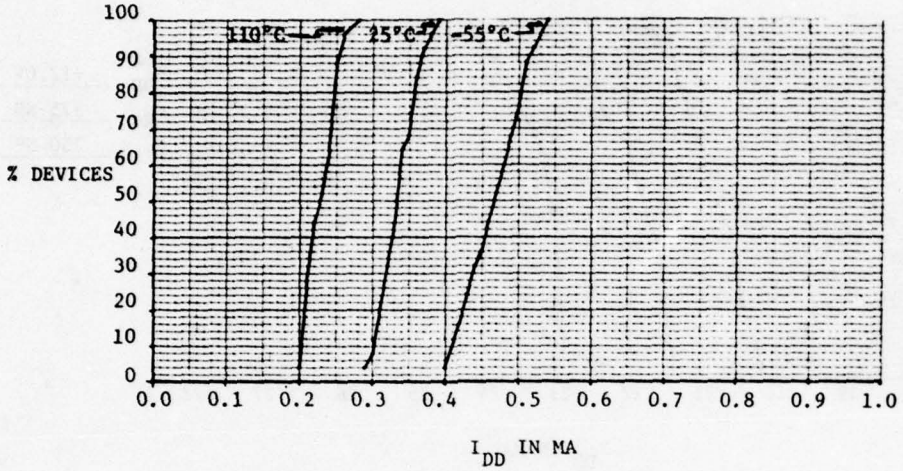
IBM)

Vendor: A
P/N:
REV: C
Date Code: 7751
25 Units

16K DYNAMIC RAM
STANDBY CURRENT
$\overline{RAS}$ & $\overline{CAS}$ INACTIVE
(HIGH)

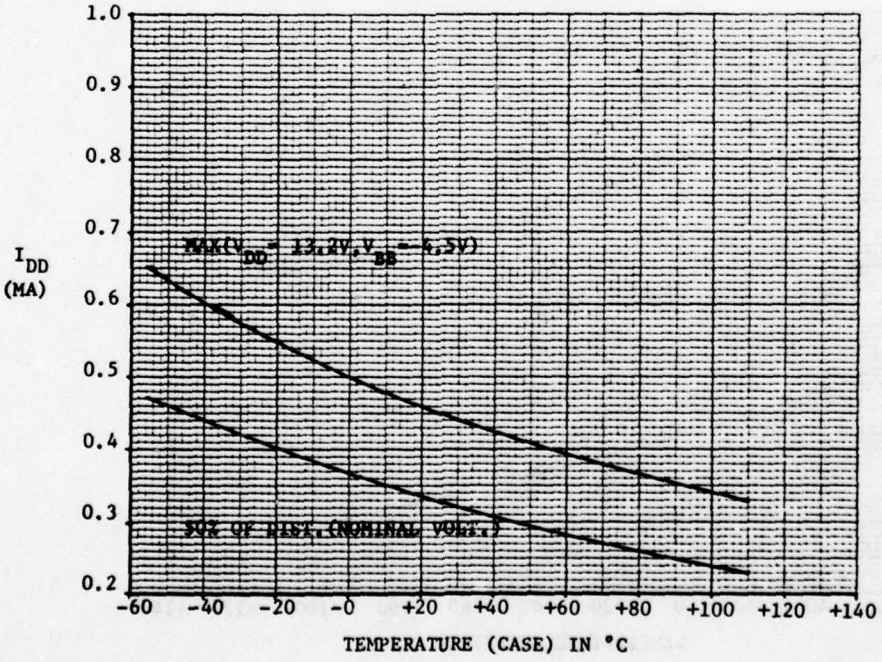
By J.R.F. Date 1/4/78
V_{BB} -5.0V V_{CC} +5.0V
LOAD N/A
ADDR PAT. N/A
DATA PAT. N/A

I_{DD2}
CUMULATIVE DISTRIBUTION



V_{DD} +12.0V

VERSUS TEMPERATURE



IBM

Vendor: A
P/N:
REV: G
Date Code: 7751
25 Units

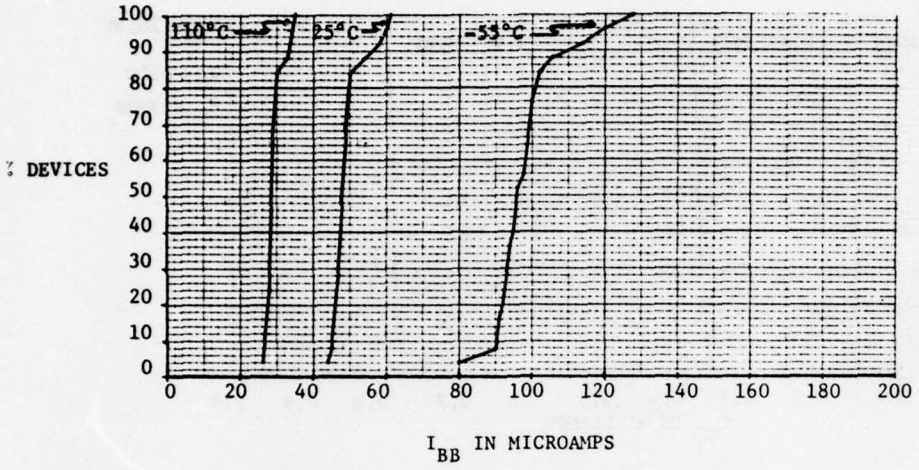
16K DYNAMIC RAM

OPERATING CURRENT

I_{BB1}

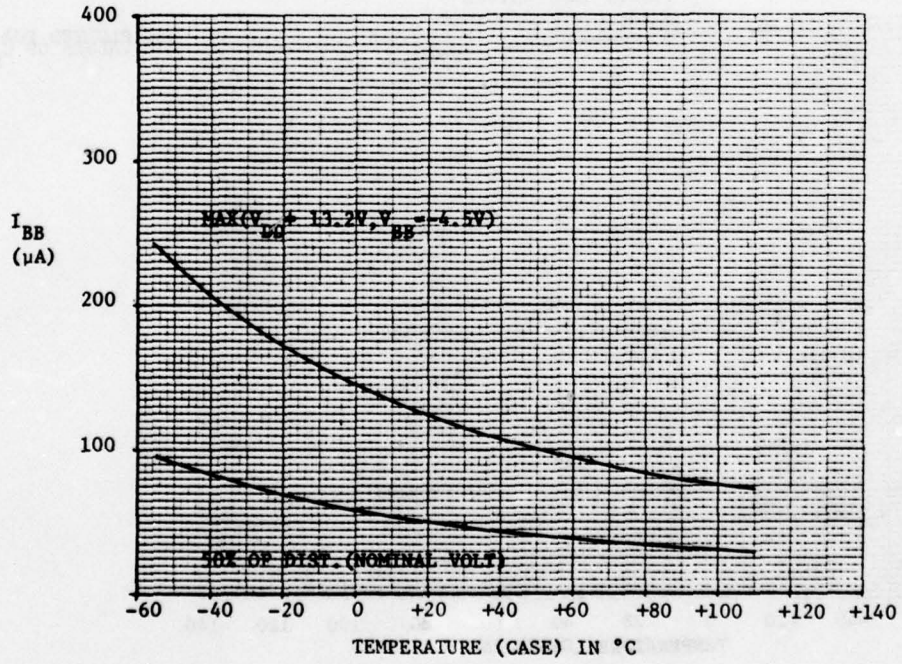
CUMULATIVE DISTRIBUTION

By J.R.F. Date 1/5/78
V_{BB} -5.0V V_{CC} +5.0V
LOAD 1 SCHOTTKY TTL + 50 pFd
ADDR PAT. WALKING DIAGONAL
DATA PAT. MAJOR DIAGONAL "1"



V_{DD} 12.0V
t_{RC} 375 ns
t_{RAS} 250 ns

VERSUS TEMPERATURE



WRT

Vendor: A
P/N:
REV: G
Date Code: 7751
DEVICES 25

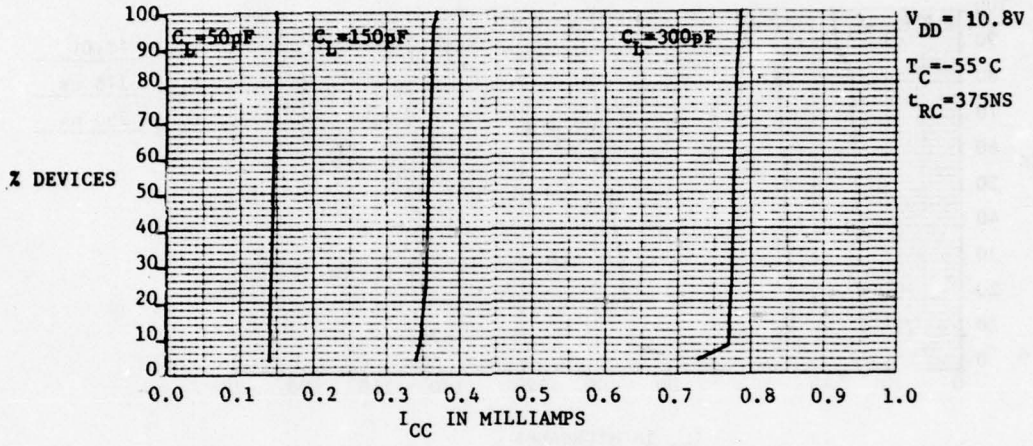
16K DYNAMIC RAM

OUTPUT DRIVER SUPPLY CURRENT

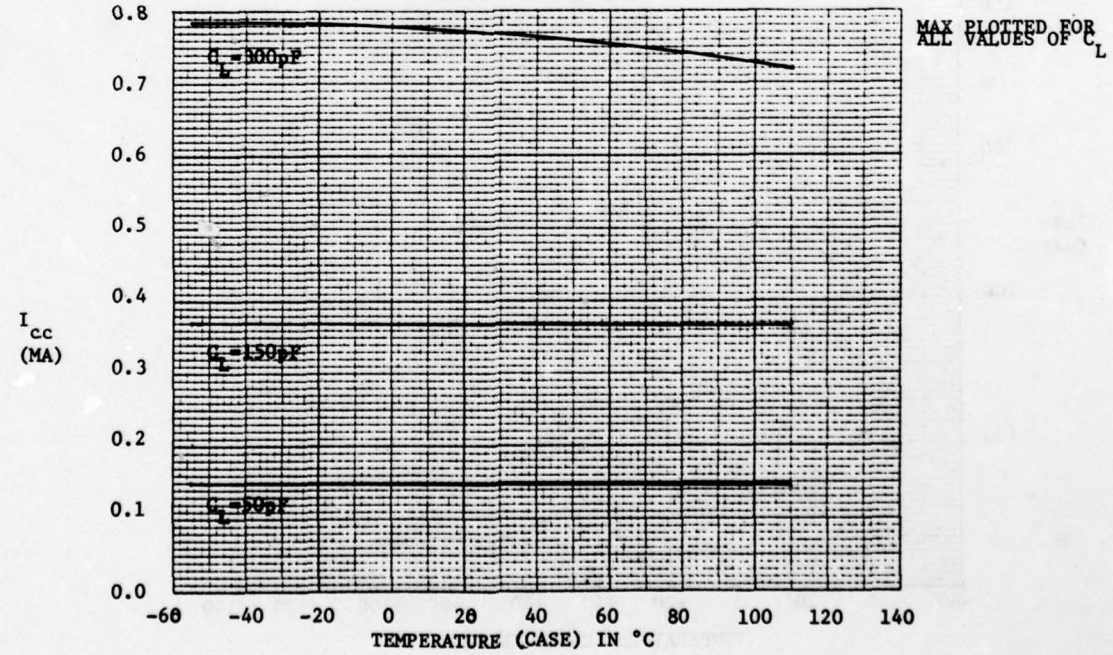
I_{CC}

By F.A.N. Date 1/20/78
V_{BB} -5.0V V_{CC} 5.0V
LOAD 1 SCHOTTKY TTL+ CL
ADDR PAT. MULTIPLE
DATA PAT. MULTIPLE

CUMULATIVE DISTRIBUTION

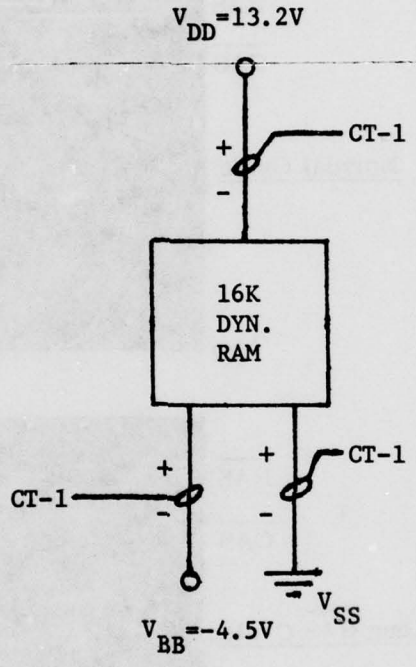


VERSUS TEMPERATURE



POWER SUPPLY TRANSIENT CURRENT

TEST SETUP



16K Dynamic RAM

Vendor: A
P/N:
Rev: G
Date Code: 7751

By: J.R.F. Date: 2/15/78

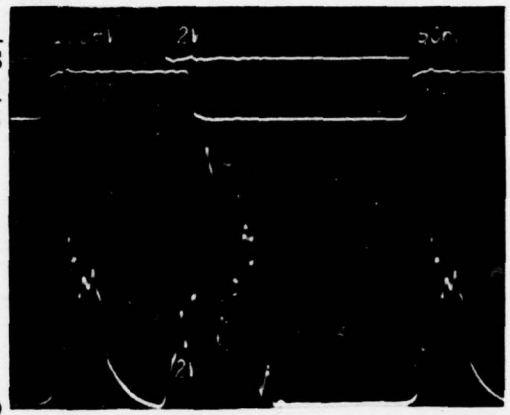
Power Supply
Transient Currents
I_{DD}

V_{DD} = 13.2 V
V_{BB} = -4.5 V
V_{CC} = 5.0 V

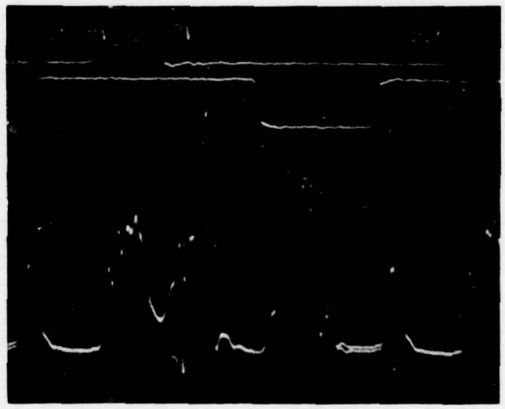
Vertical: $\overline{RAS}$ & $\overline{CAS}$ =2 V/cm
I_{DD} =20 mA/cm
Horizontal: 50 ns/cm

T_{case} = 25°C

Normal Cycle



Long $\overline{RAS}$ Cycle



$\overline{RAS}$ only Cycle

16K Dynamic RAM

Vendor: A
P/N:
Rev: G
Date Code: 7751

By: J.R.F. Date: 2/15/78

Power Supply
Transient Currents
I_{DD}

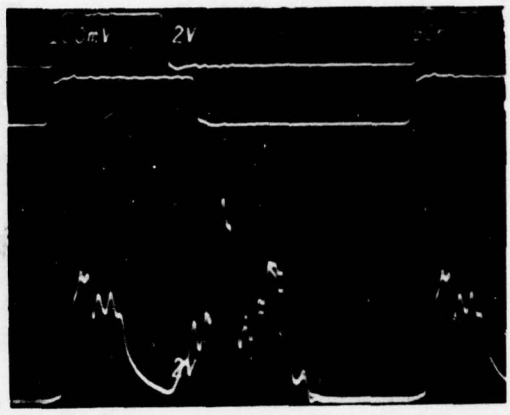
V_{DD} = 13.2 V
V_{BB} = -4.5 V
V_{CC} = 5.0 V

Vertical: $\overline{RAS}$ & $\overline{CAS}$ =2 V/cm
I_{DD} = 20 mA/cm

Horizontal: =50 ns/cm

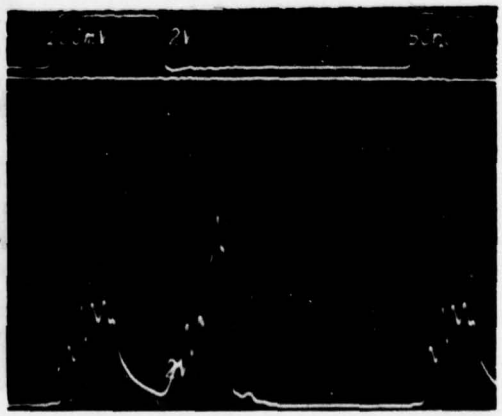
T_{case}=110°C

Normal Cycle



Long RAS Cycle

RAS only Cycle



16K Dynamic RAM

Vendor: A
P/N:
Rev: G
Date Code: 7751

By: J.R.F. Date: 2/15/78

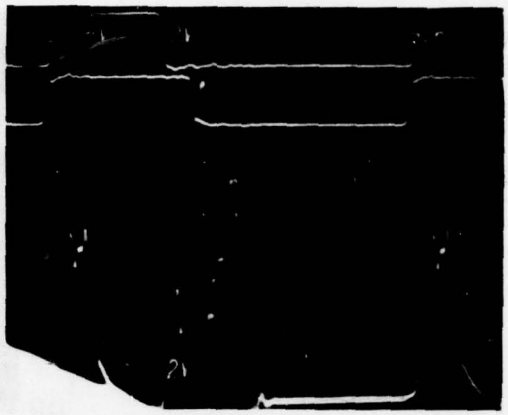
Power Supply
Transient Currents
I_{DD}

V_{DD} = 13.2 V
V_{BB} = -4.5 V
V_{CC} = 5.0 V

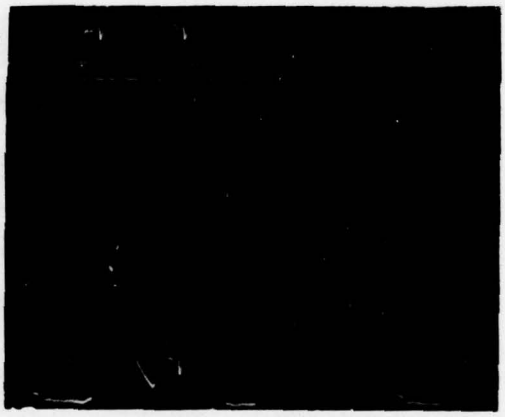
Vertical: $\overline{RAS}$ & $\overline{CAS}$ =2 V/cm
I_{DD} =20 mA/cm
Horizontal: 50 ns/cm

T_{case} =-55°C

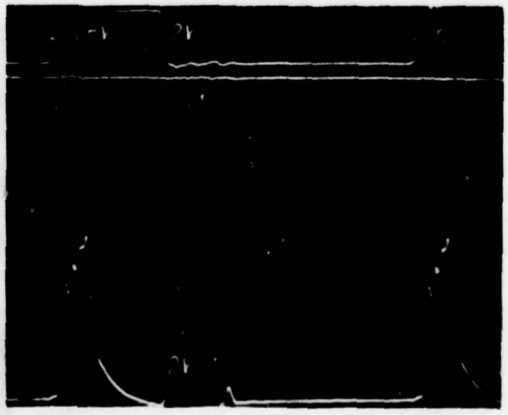
Normal Cycle



Long $\overline{RAS}$ Cycle



$\overline{RAS}$ only Cycle



16K Dynamic RAM

Vendor: A
P/N:
Rev: G
Date Code: 7751

By: J.R.F. Date: 2/15/78

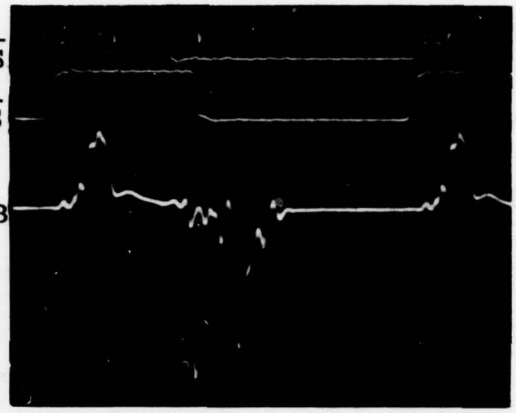
Power Supply
Transient Currents
I_{BB}

V_{DD} = 13.2 V
V_{BB} = -4.5 V
V_{CC} = 5.0 V

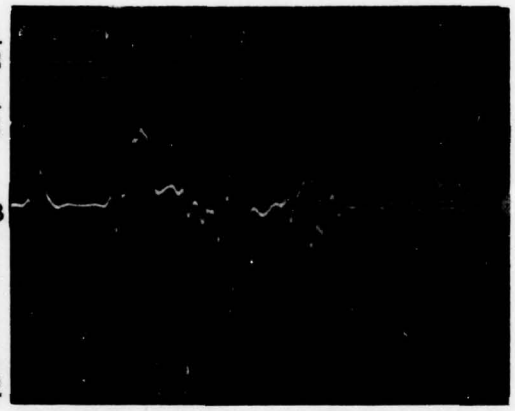
Vertical: $\overline{RAS}$ & $\overline{CAS}$ = 2 V/cm
I_{BB} = 20 mA/cm

Horizontal: 50 ns/cm

T_{case} = 25°C



Normal Cycle



Long $\overline{RAS}$ Cycle

$\overline{RAS}$ only Cycle

16K Dynamic RAM

Vendor: A
P/N:
Rev: G
Date Code: 7751

By: J.R.F. Date: 2/15/78

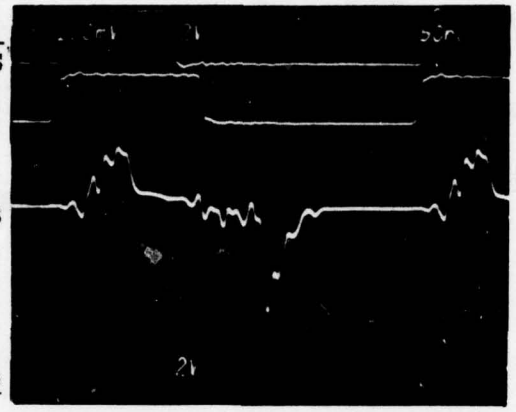
Power Supply Transient Currents
I_{BB}

V_{DD} = 13.2 V
V_{BB} = -4.5 V
V_{CC} = 5.0 V

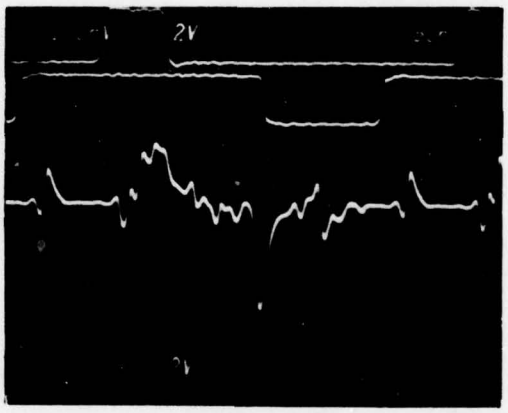
Vertical: $\overline{RAS}$ & $\overline{CAS}$ = 2 V/cm
I_{BB} = 20 mA/cm

Horizontal: 50 ns/cm

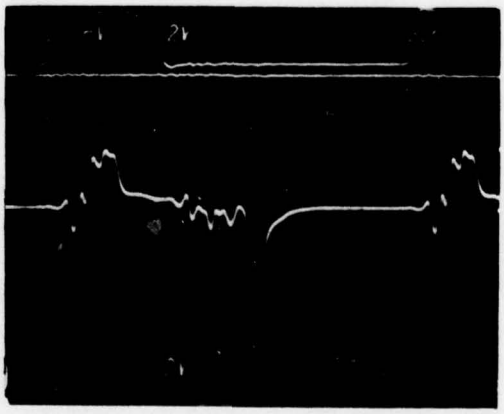
T_{case} = 110°C



Normal Cycle



Long $\overline{RAS}$ Cycle



$\overline{RAS}$ only Cycle

16K Dynamic RAM

Vendor: A
P/N:
Rev: G
Date Code: 7751

By: J.R.F. Date: 2/15/78

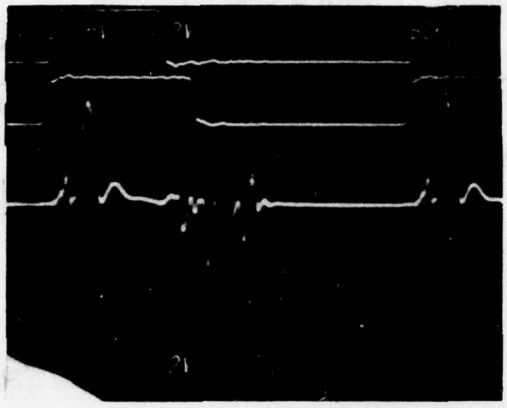
Power Supply
Transient Currents
I_{BB}

V_{DD} = 13.2 V
V_{BB} = -4.5 V
V_{CC} = 5.0 V

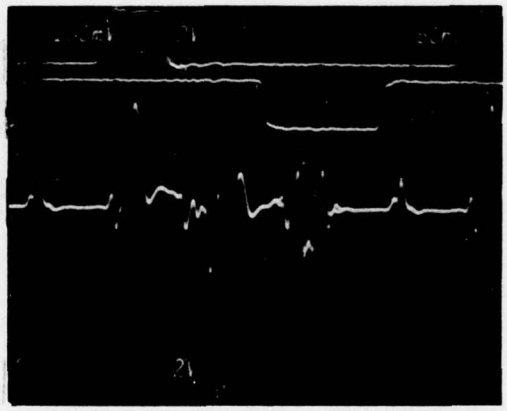
Vertical: $\overline{RAS}$ & $\overline{CAS}$ = 2 V/cm
I_{SS} = 20 mA/cm

Horizontal: 50 ns/cm

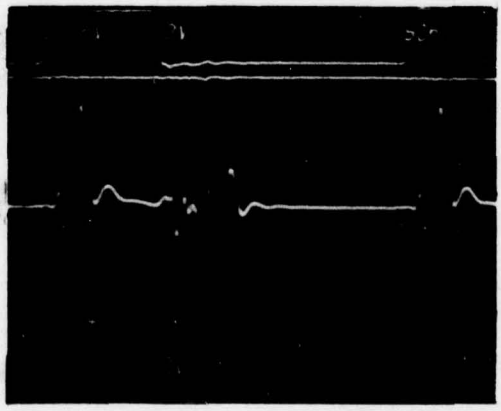
T_{case} = -55°C



Normal Cycle



Long $\overline{RAS}$ Cycle



$\overline{RAS}$ only Cycle

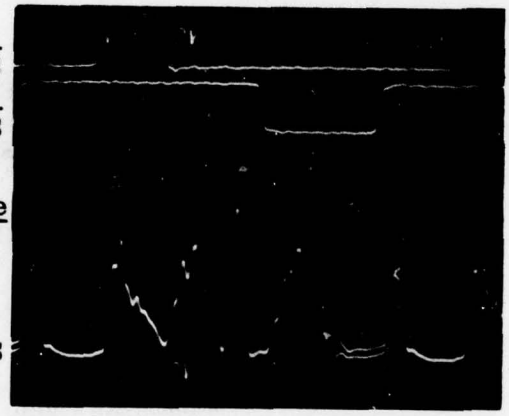
16K Dynamic RAM

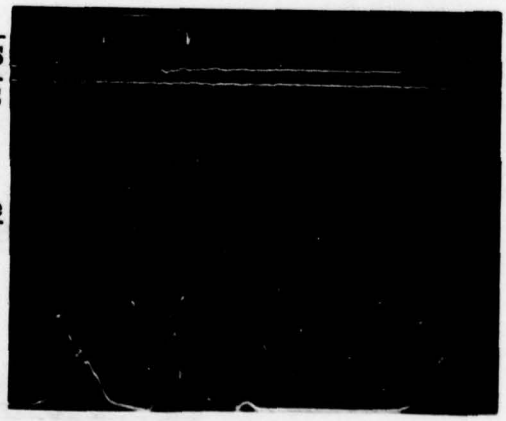
Vendor: A
P/N:
Rev: G
Date Code: 7751

Power Supply
Transient Currents
I_{SS}

By: J.R.F. Date: 2/15/78
V_{DD} = 13.2 V
V_{BB} = -4.5 V
V_{CC} = 5.0 V

Vertical: RAS & CAS = 2 V/cm
I_{SS} = 20 mA/cm
Horizontal: 50 ns/cm
T_{case} = 25°C





16K Dynamic RAM

Vendor: A
P/N:
Rev: G
Date Code: 7751

By: J.R.F. Date: 2/15/78

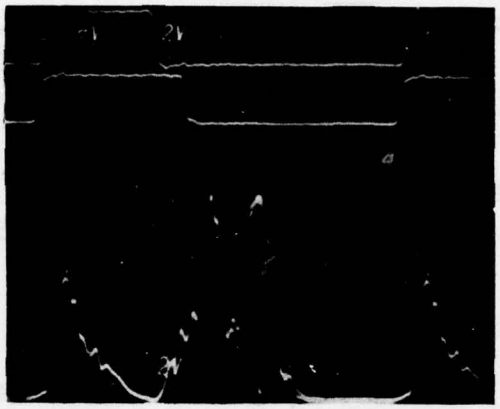
Power Supply
Transient Currents
I_{SS}

V_{DD} = 13.2 V
V_{BB} = -4.5 V
V_{CC} = 5.0 V

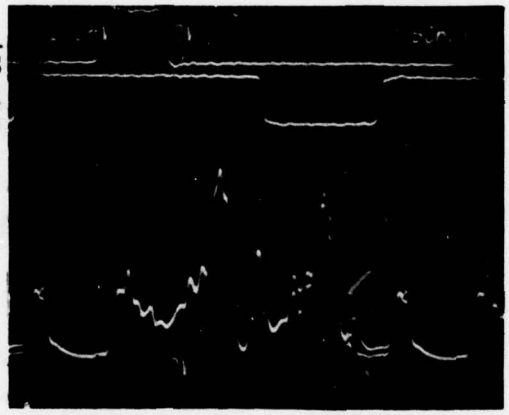
Vertical: $\overline{RAS}$ & $\overline{CAS}$ = 2 V/cm
I_{SS} = 20 mA/cm
Horizontal: 50 ns/cm

T_{case} = 110°C

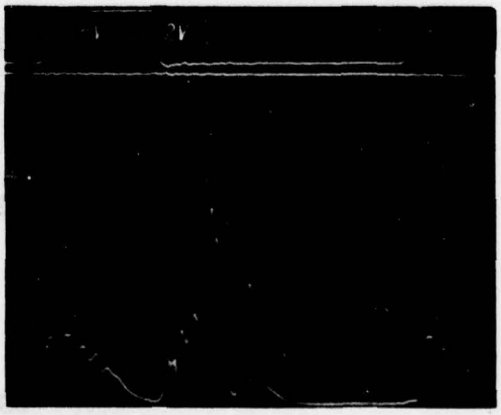
$\overline{RAS}$
$\overline{CAS}$
Normal Cycle
I_{SS}



$\overline{RAS}$
$\overline{CAS}$
Long $\overline{RAS}$ Cycle
I_{SS}



$\overline{RAS}$
$\overline{CAS}$
$\overline{RAS}$ only Cycle
I_{SS}



16K Dynamic RAM

Vendor: A
P/N:
Rev: G
Date Code: 7751

By: J.R.F. Date: 2/15/78

Power Supply
Transient Currents
I_{SS}

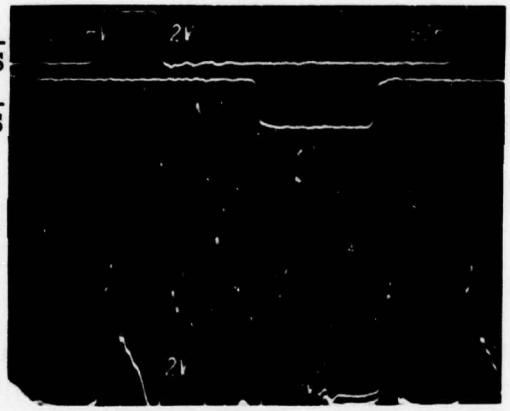
V_{DD} = 13.2 V
V_{BB} = -4.5 V
V_{CC} = 5.0 V

Vertical: $\overline{RAS}$ & $\overline{CAS}$ = 2 V/cm
I_{BB} = 20 mA/cm
Horizontal: 50 ns/cm

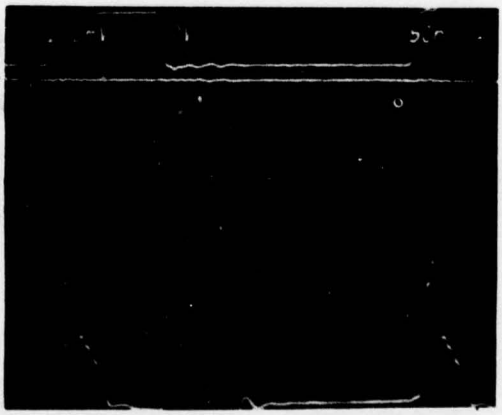
T_{case} = -55°C

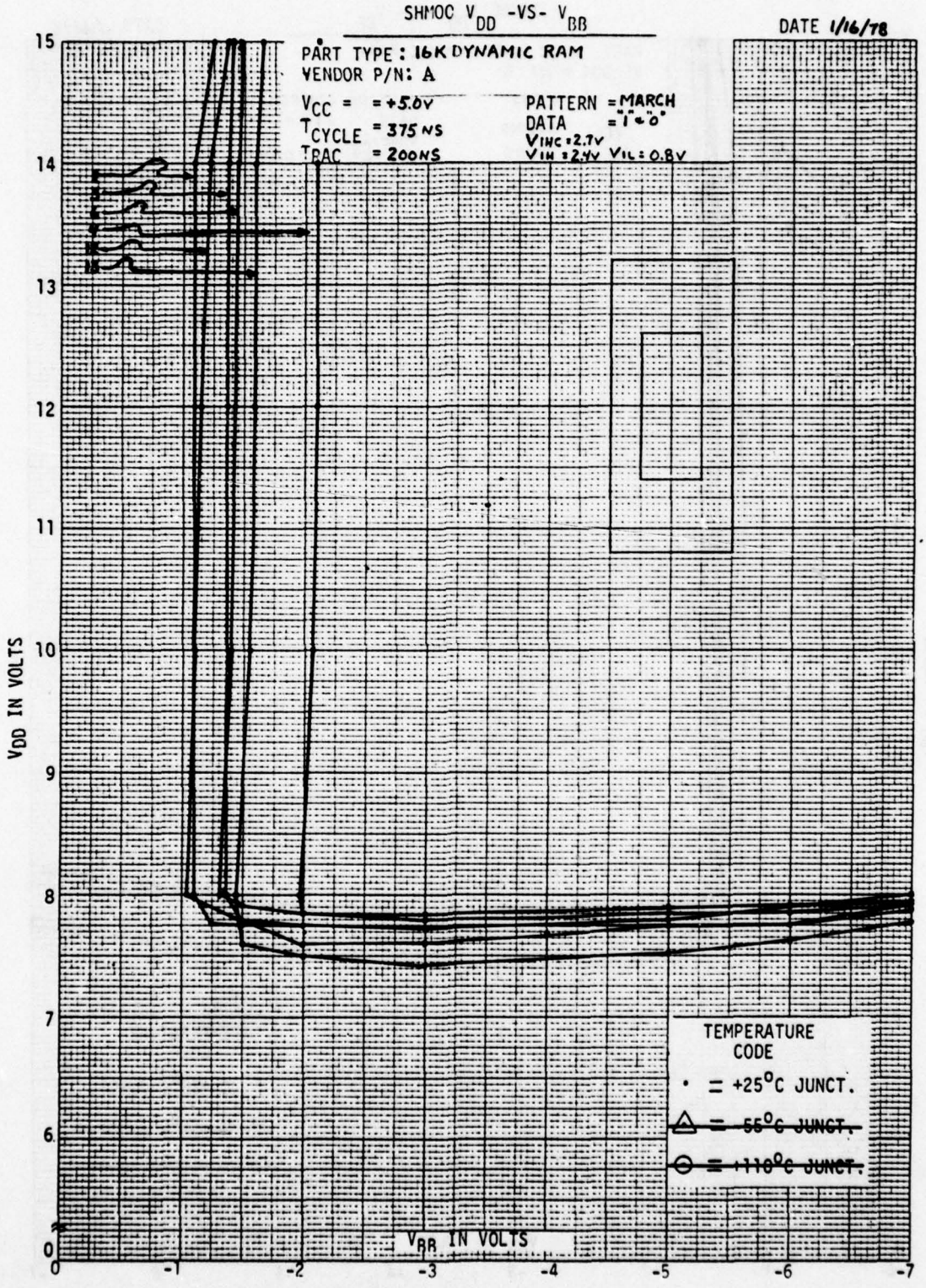
Normal Cycle

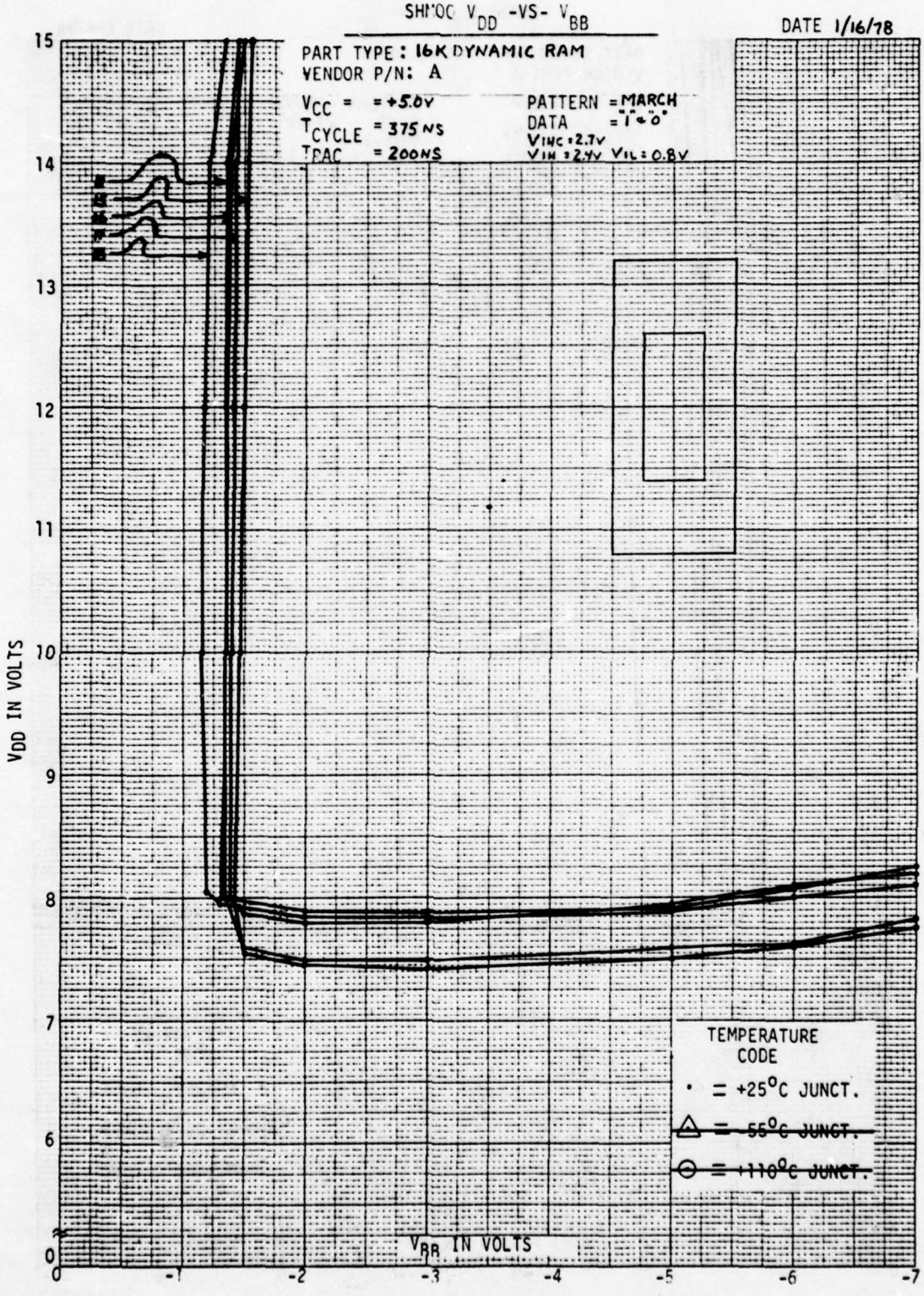
Long $\overline{RAS}$ Cycle

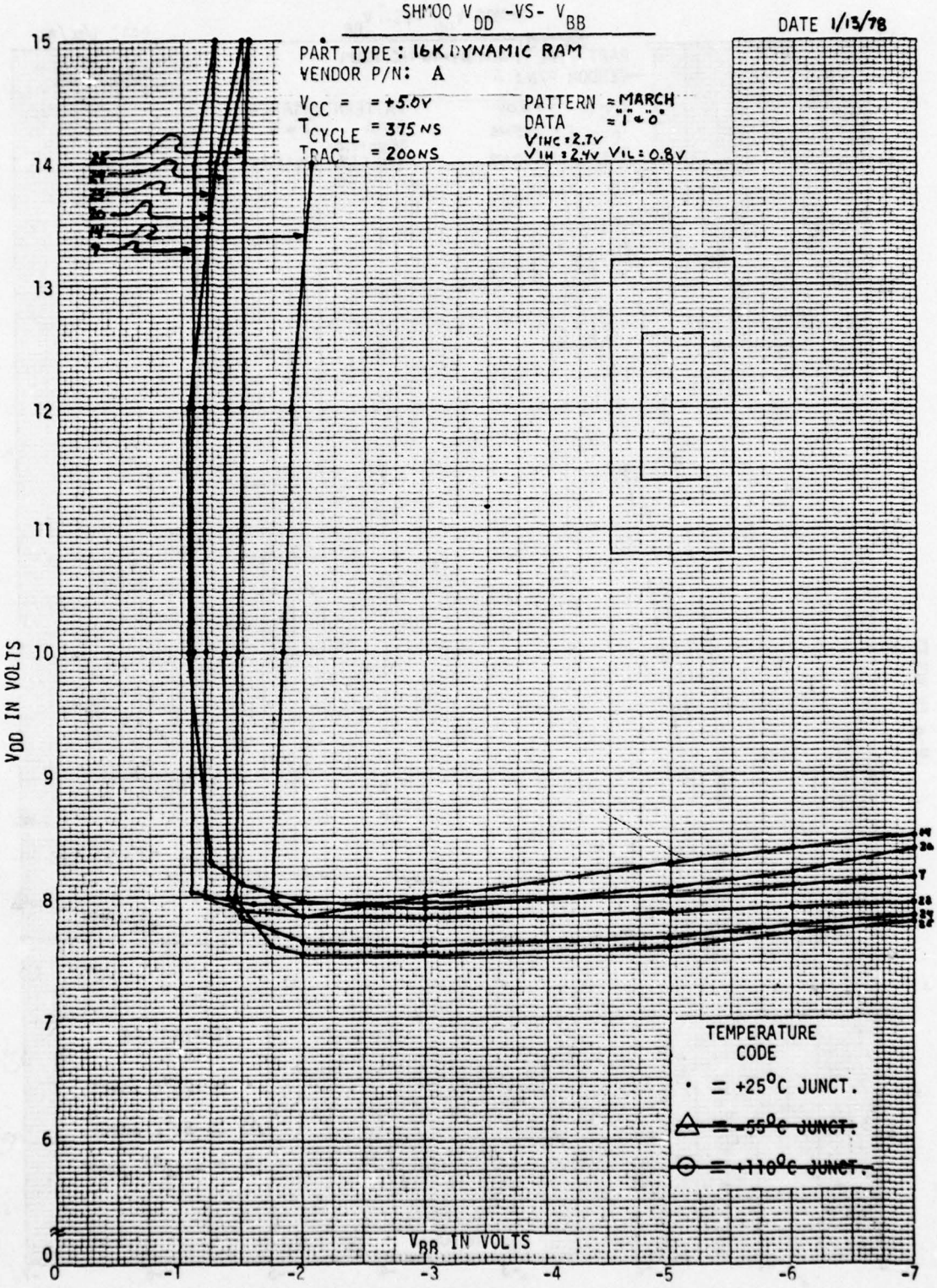


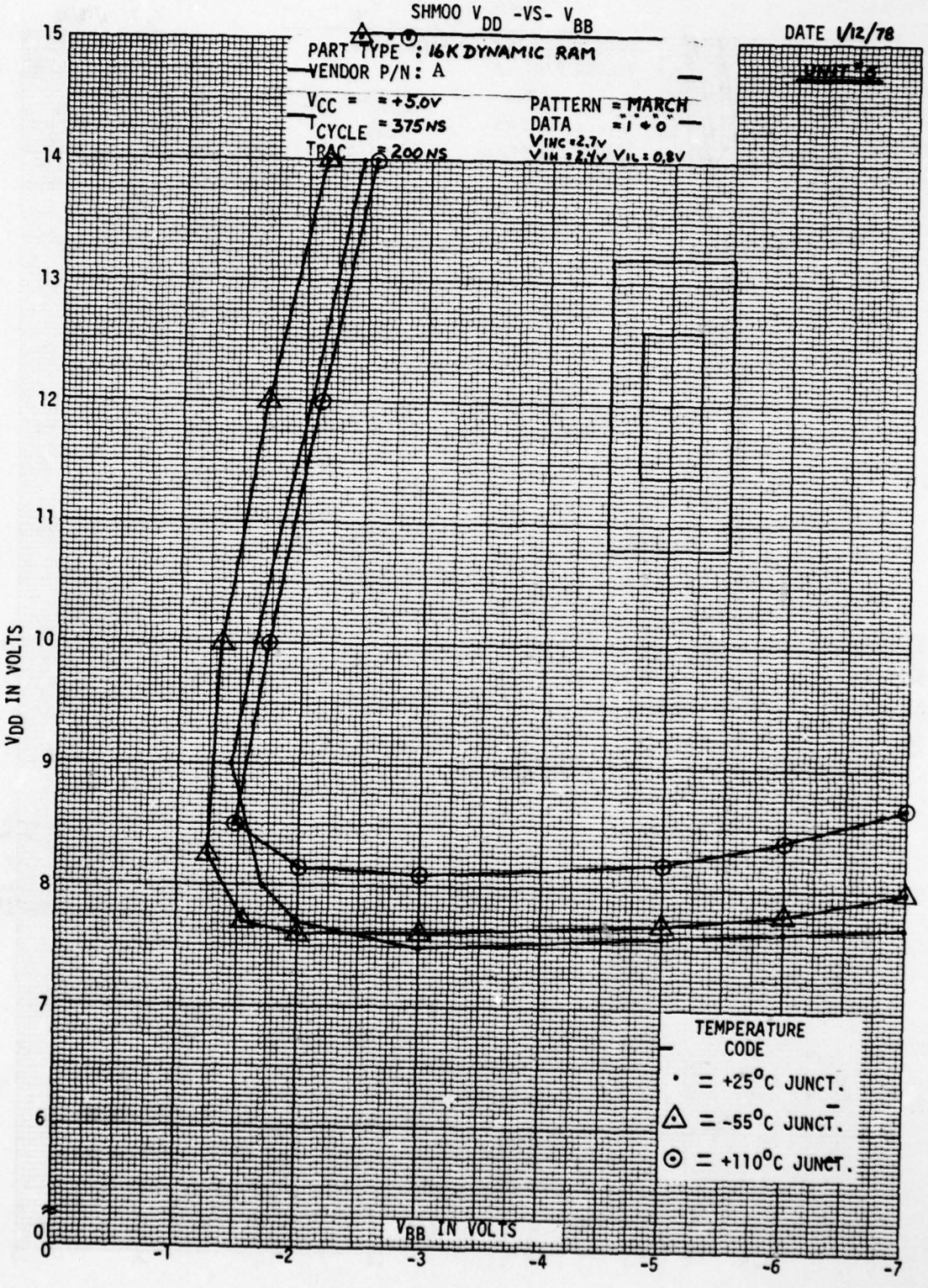
$\overline{RAS}$ only Cycle

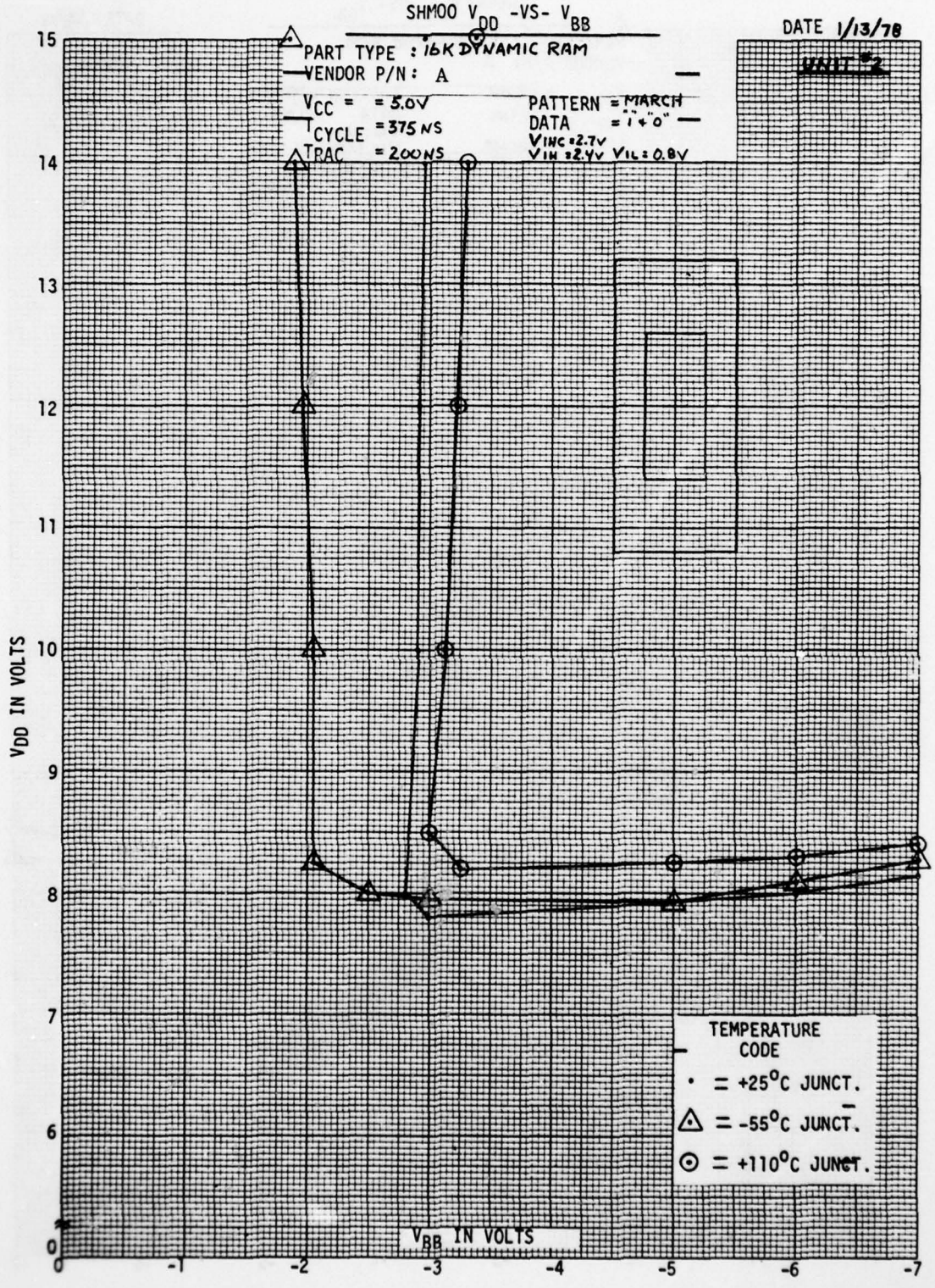


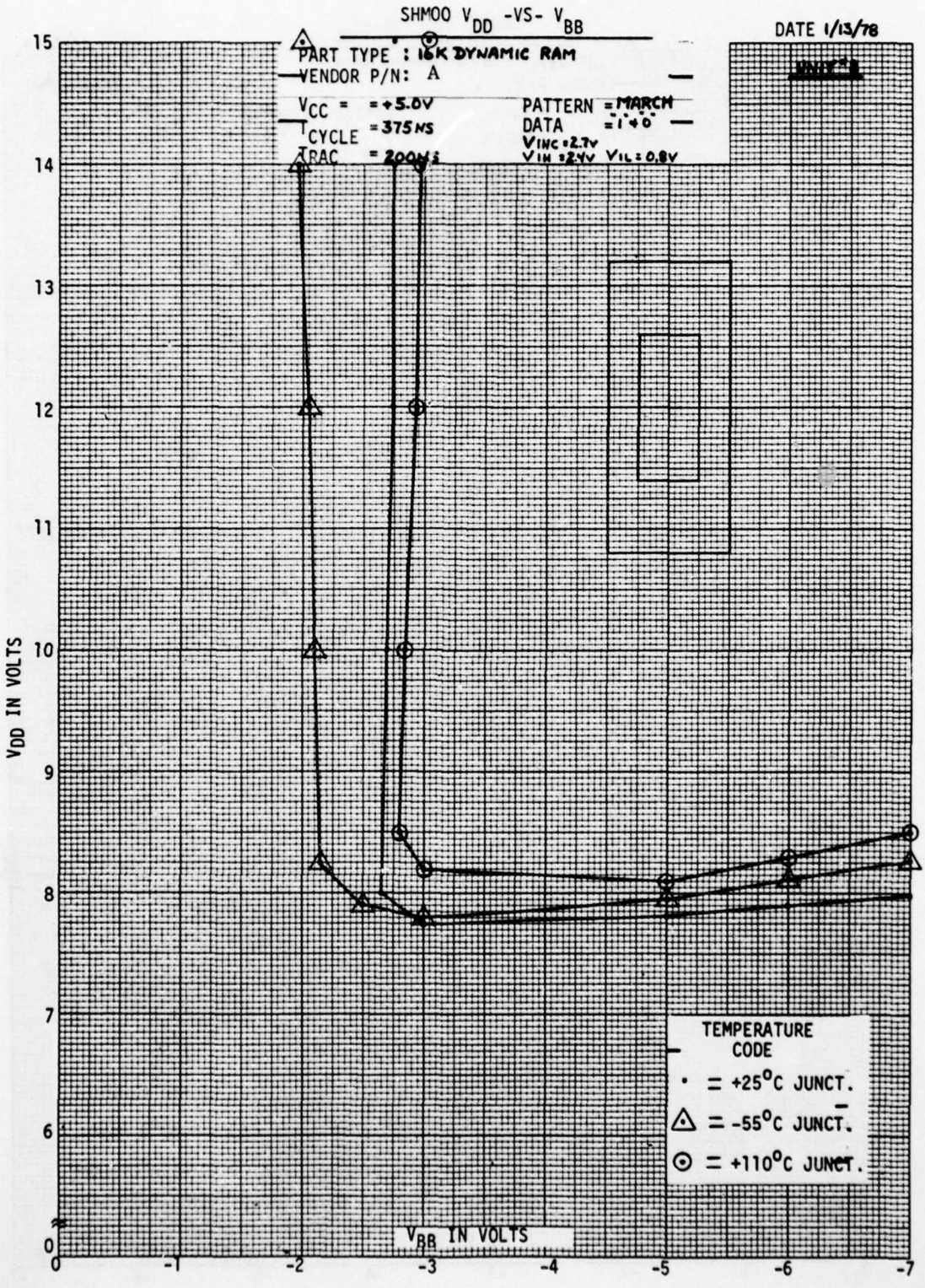

SHMOO V_{DD} -VS- V_{BB}
DATE 1/16/78
PART TYPE: 16K DYNAMIC RAM
VENDOR P/N: A
V_{CC} = +5.0V
T_{CYCLE} = 375 NS
T_{RAC} = 200NS
PATTERN = MARCH
DATA = "1" & "0"
V_{INC} = 2.7V
V_{IH} = 2.4V V_{IL} = 0.8V
V_{DD} IN VOLTS
V_{BB} IN VOLTS
TEMPERATURE CODE
• = +25°C JUNCT.
△ = 55°C JUNCT.
○ = +110°C JUNCT.

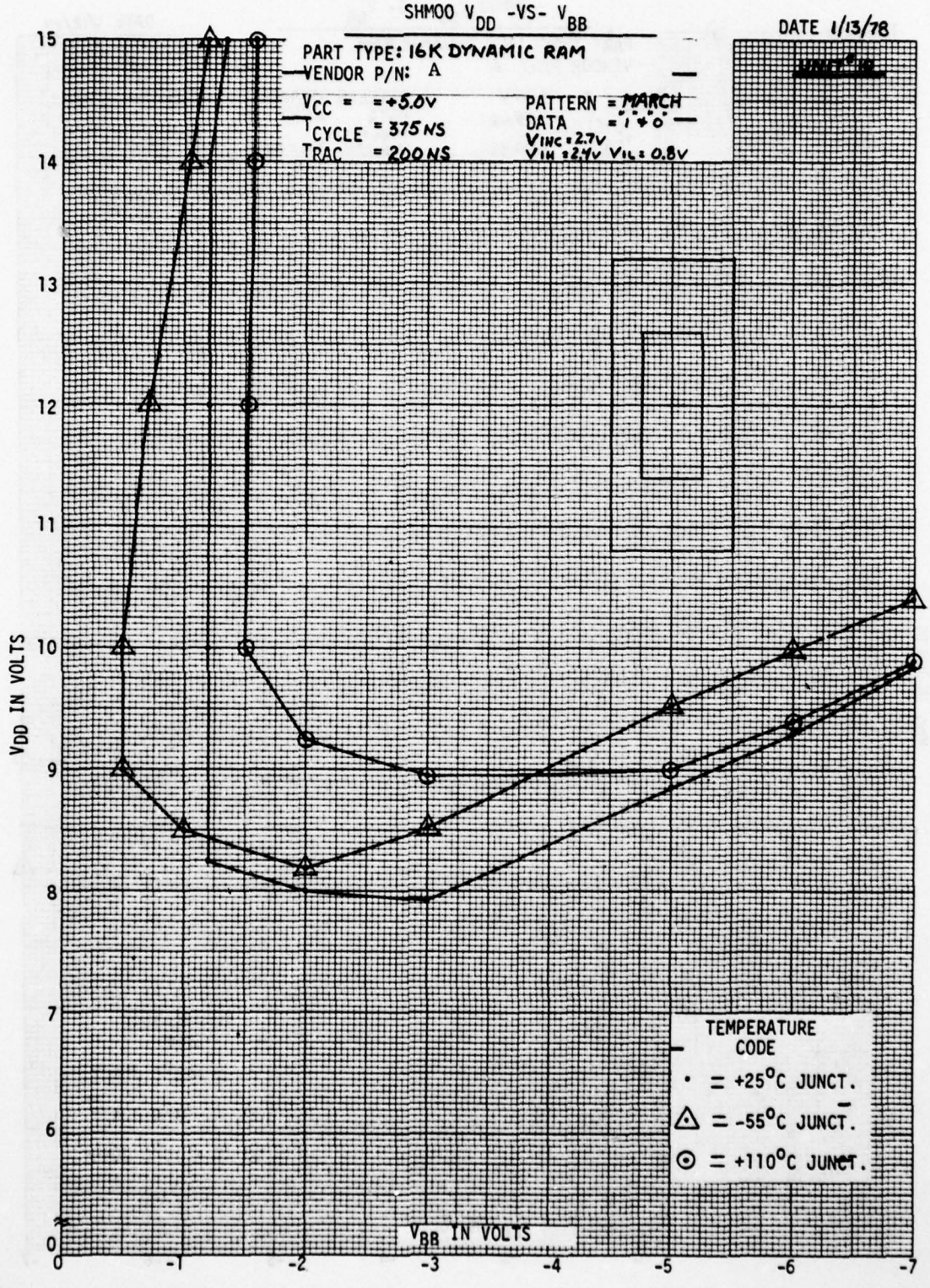

SHMOO V_{DD} -VS- V_{BB}
DATE 1/16/78
PART TYPE: 16K DYNAMIC RAM
VENDOR P/N: A
V_{CC} = +5.0V
T_{CYCLE} = 375 NS
T_{RAC} = 200NS
PATTERN = MARCH
DATA = "1" & "0"
V_{INC} = 2.7V
V_{IH} = 2.4V V_{IL} = 0.8V
V_{DD} IN VOLTS
V_{BB} IN VOLTS
TEMPERATURE CODE
· = +25°C JUNCT.
△ = -55°C JUNCT.
○ = +110°C JUNCT.

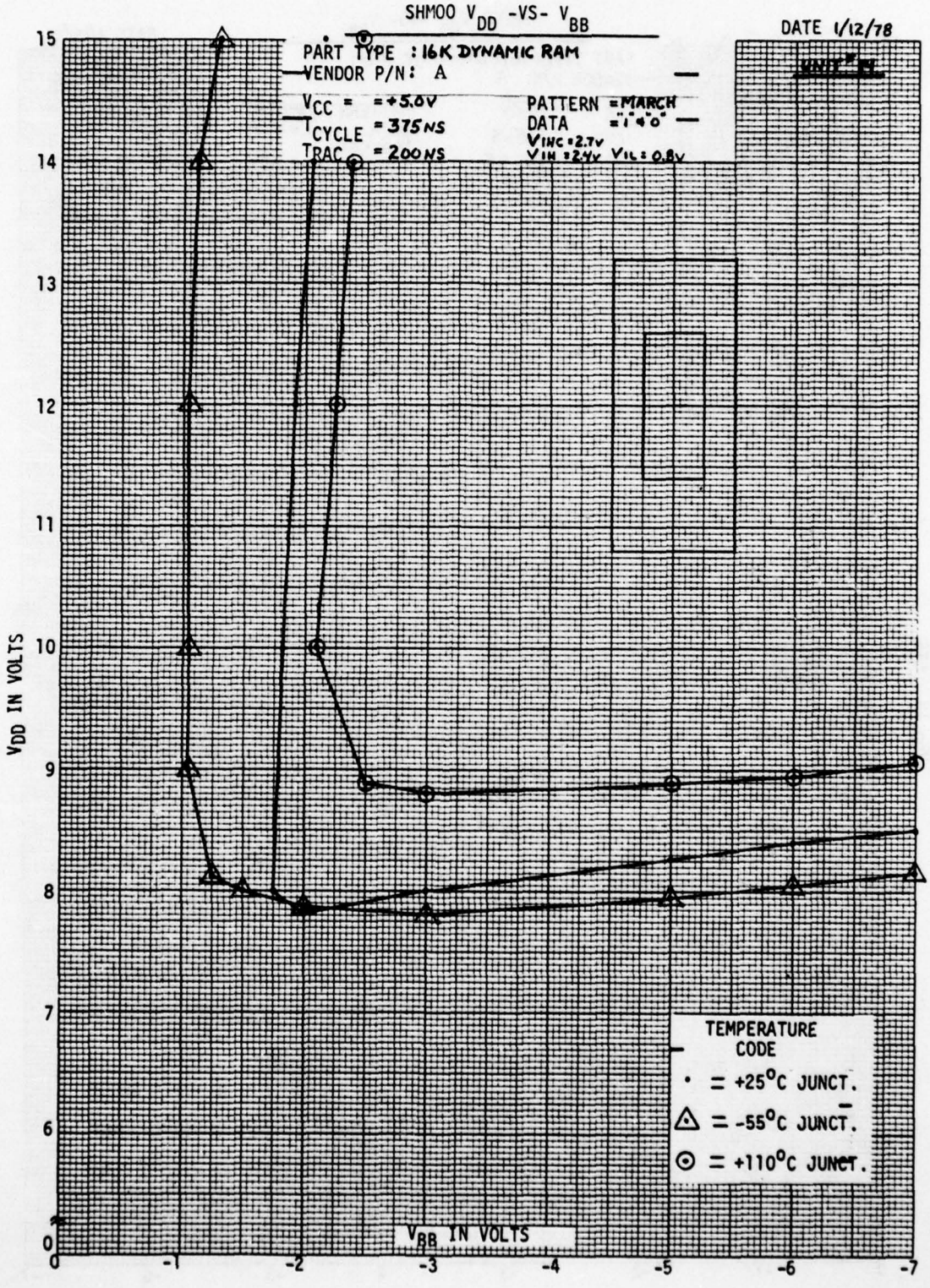

SHMOO V_{DD} -VS- V_{BB}
DATE 1/13/78
PART TYPE: 16K DYNAMIC RAM
VENDOR P/N: A
V_{CC} = +5.0V
T_{CYCLE} = 375 NS
T_{RAC} = 200NS
PATTERN = MARCH
DATA = "1" & "0"
V_{IHC} = 2.7V
V_{IH} = 2.4V V_{IL} = 0.8V
V_{DD} IN VOLTS
V_{BB} IN VOLTS
TEMPERATURE CODE
• = +25°C JUNCT.
△ = -55°C JUNCT.
○ = +110°C JUNCT.

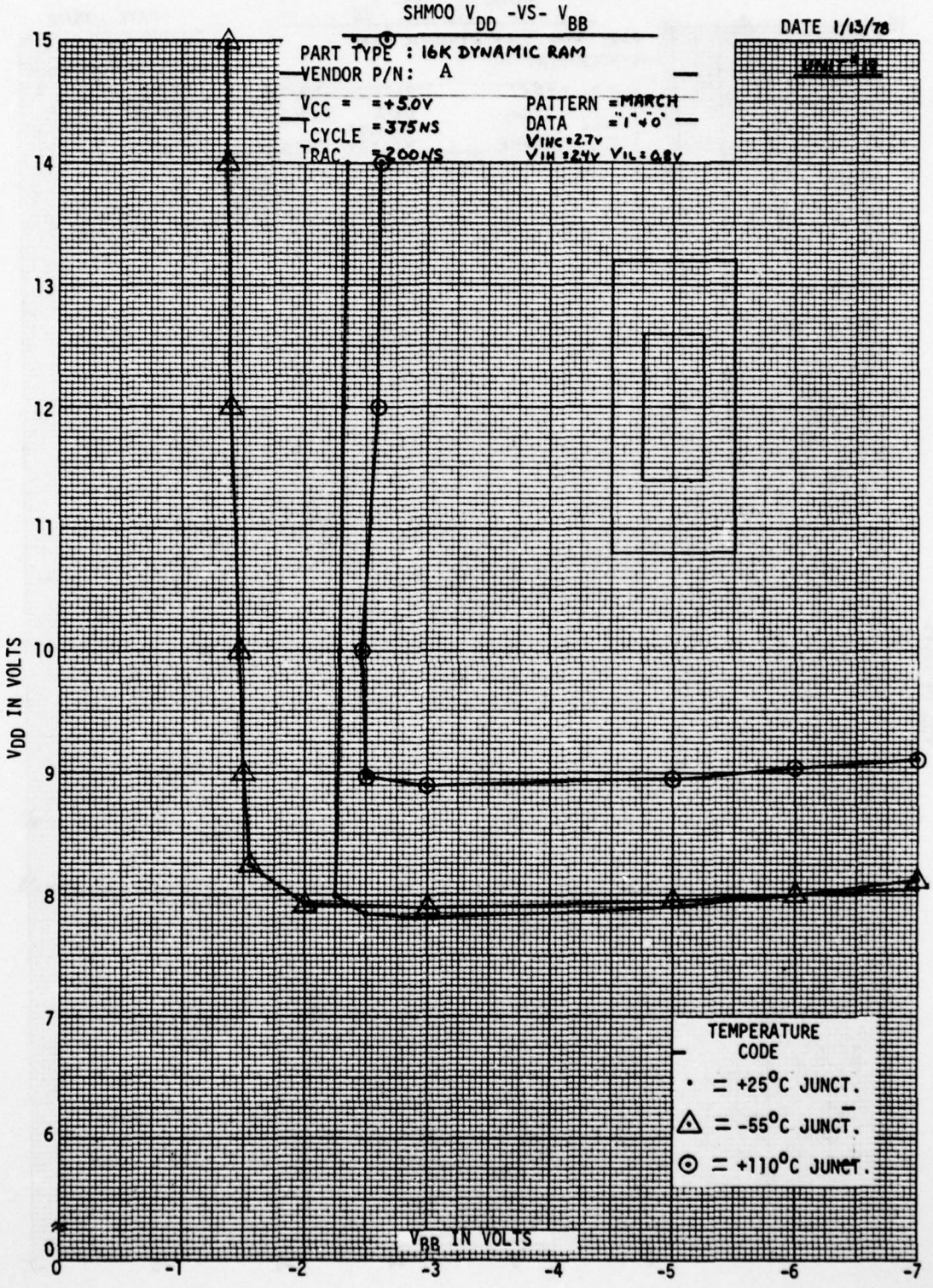

SHMOO V_{DD} -VS- V_{BB}
DATE 1/12/78
PART TYPE : 16K DYNAMIC RAM
VENDOR P/N: A
V_{CC} = +5.0V
T_{CYCLE} = 375 NS
T_{RAC} = 200 NS
PATTERN = MARCH
DATA = "1" & "0"
V_{INC} = 2.7V
V_{IH} = 2.4V V_{IL} = 0.8V
V_{DD} IN VOLTS
V_{BB} IN VOLTS
TEMPERATURE CODE
• = +25°C JUNCT.
△ = -55°C JUNCT.
⊙ = +110°C JUNCT.

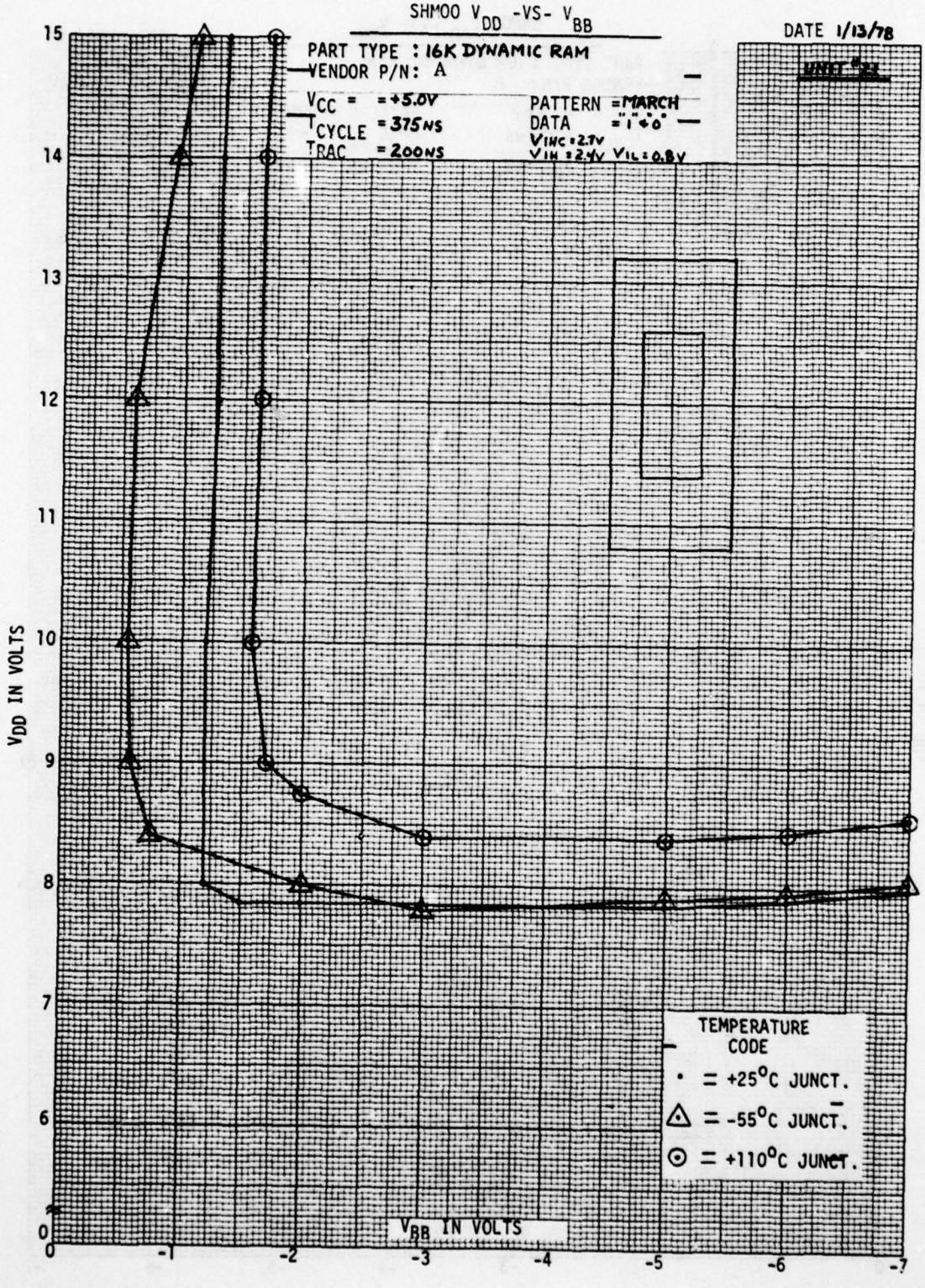

SHMOO V_{DD} -VS- V_{BB}
DATE 1/13/78
PART TYPE : 16K DYNAMIC RAM
VENDOR P/N : A
UNIT #2
V_{CC} = = 5.0V
T_{CYCLE} = 375 NS
T_{RAC} = 200NS
PATTERN = MARCH
DATA = "1" + "0"
V_{IHC} = 2.7V
V_{IH} = 2.4V V_{IL} = 0.8V
V_{DD} IN VOLTS
V_{BB} IN VOLTS
TEMPERATURE CODE
• = +25°C JUNCT.
△ = -55°C JUNCT.
⊙ = +110°C JUNCT.
15
14
13
12
11
10
9
8
7
6
0
0
-1
-2
-3
-4
-5
-6
-7


SHMOO V_{DD} -VS- V_{BB}
DATE 1/13/78
PART TYPE : 16K DYNAMIC RAM
VENDOR P/N: A
V_{CC} = +5.0V
T_{CYCLE} = 375 NS
T_{RAC} = 200 NS
PATTERN = MARCH
DATA = 1 0
V_{IHC} = 2.7V
V_{IH} = 2.4V V_{IL} = 0.8V
V_{DD} IN VOLTS
V_{BB} IN VOLTS
TEMPERATURE CODE
• = +25°C JUNCT.
△ = -55°C JUNCT.
⊙ = +110°C JUNCT.
15
14
13
12
11
10
9
8
7
6
0
0
-1
-2
-3
-4
-5
-6
-7


SHMOO V_{DD} -VS- V_{BB}
DATE 1/13/78
PART TYPE: 16K DYNAMIC RAM
VENDOR P/N: A
V_{CC} = +5.0V
T_{CYCLE} = 375 NS
T_{RAC} = 200 NS
PATTERN = MARCH
DATA = 1 + 0
V_{INC} = 2.7V
V_{IH} = 2.4V V_{IL} = 0.8V
V_{DD} IN VOLTS
V_{BB} IN VOLTS
TEMPERATURE CODE
• = +25°C JUNCT.
△ = -55°C JUNCT.
⊙ = +110°C JUNCT.


SHMOO V_{DD} -VS- V_{BB}
DATE 1/12/78
PART TYPE : 16K DYNAMIC RAM
VENDOR P/N: A
V_{CC} = +5.0V
T_{CYCLE} = 375 NS
T_{RAC} = 200 NS
PATTERN = MARCH
DATA = "1" "0"
V_{INC} = 2.7V
V_{IH} = 2.4V V_{IL} = 0.8V
V_{DD} IN VOLTS
V_{BB} IN VOLTS
TEMPERATURE CODE
• = +25°C JUNCT.
△ = -55°C JUNCT.
⊙ = +110°C JUNCT.


SHMOO V_{DD} -VS- V_{BB}
DATE 1/13/78
PART TYPE : 16K DYNAMIC RAM
VENDOR P/N: A
V_{CC} = =+5.0V
T_{CYCLE} =375NS
T_{RAC} =200NS
PATTERN =MARCH
DATA ="1"+"0"
V_{INC} =2.7V
V_{IH} =2.4V V_{IL} =0.8V
V_{DD} IN VOLTS
V_{BB} IN VOLTS
TEMPERATURE CODE
• = +25°C JUNCT.
△ = -55°C JUNCT.
⊙ = +110°C JUNCT.


SHMOO V_{DD} -VS- V_{BB}
DATE 1/13/78
PART TYPE : 16K DYNAMIC RAM
VENDOR P/N: A
UNIT #21
V_{CC} = +5.0V
T_{CYCLE} = 375NS
T_{RAC} = 200NS
PATTERN = MARCH
DATA = "1" & "0"
V_{IHC} = 2.7V
V_{IH} = 2.4V V_{IL} = 0.8V
V_{DD} IN VOLTS
V_{BB} IN VOLTS
TEMPERATURE CODE
• = +25°C JUNCT.
△ = -55°C JUNCT.
⊙ = +110°C JUNCT.
15
14
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7
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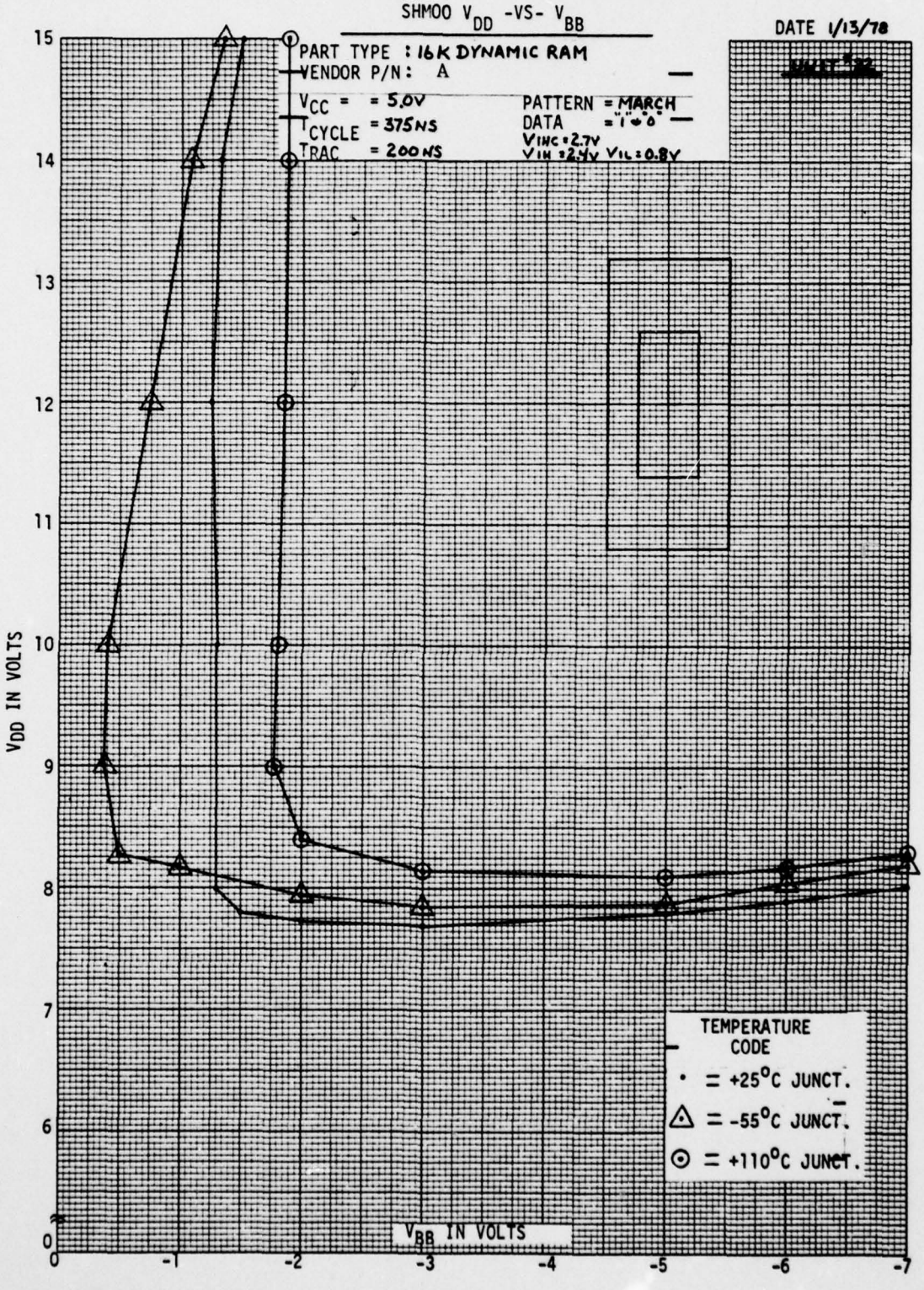
0
-1
-2
-3
-4
-5
-6
-7


SHMOO V_{DD} -VS- V_{BB}
DATE 1/13/78
PART TYPE : 16K DYNAMIC RAM
VENDOR P/N: A
V_{CC} = = 5.0V
T_{CYCLE} = 375NS
T_{RAC} = 200NS
PATTERN = MARCH
DATA = "1" & "0"
V_{INC} = 2.7V
V_{IH} = 2.4V V_{IL} = 0.8V
V_{DD} IN VOLTS
V_{BB} IN VOLTS
TEMPERATURE CODE
• = +25°C JUNCT.
△ = -55°C JUNCT.
⊙ = +110°C JUNCT.
15
14
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-2
-3
-4
-5
-6
-7

APPENDIX II

16K DYNAMIC RAM

VENDOR B

Vendor: B
P/N:
REV: (Shrink)
Date Code: 7820
Device: 27

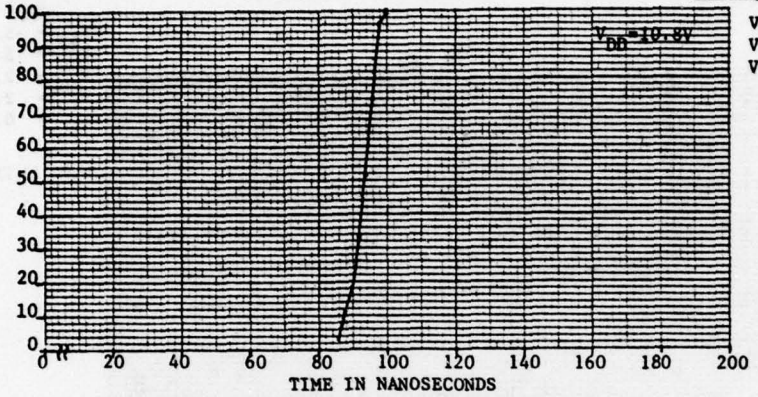
16K DYNAMIC RAM

ACCESS TIME FROM $\overline{CAS}$

t_{CAC}

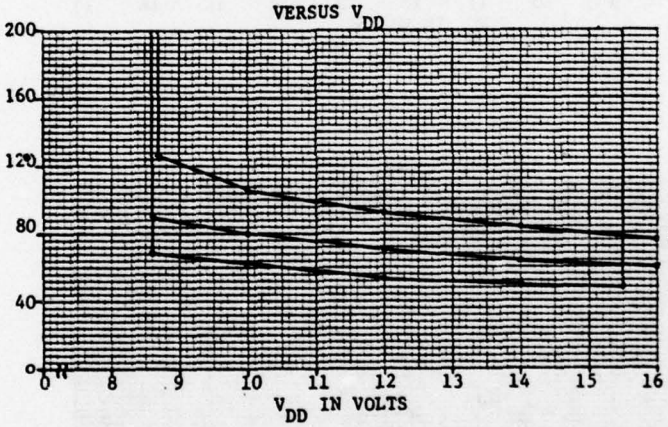
By J.R.F. Date 6/13/78
V_{BB} -4.5V V_{CC} 5.0V
LOAD 1 Schottky TTL + 50pF
ADDR PAT. Multiple
DATA PAT. Multiple

CUMULATIVE DISTRIBUTION

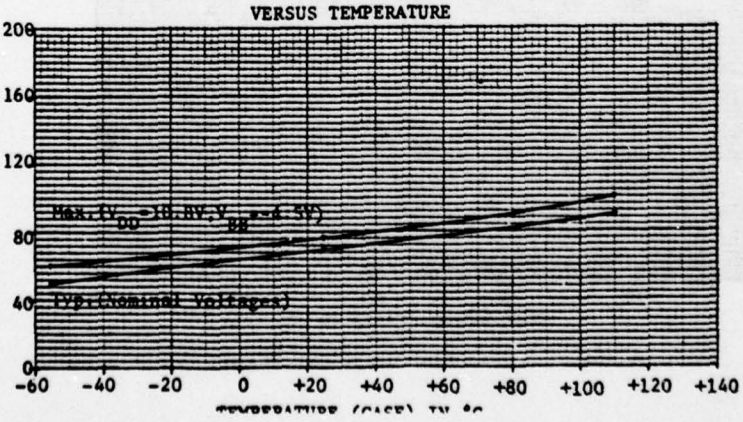


VIHC 2.7V
VIH 2.4V
VIL 0.8V

VERSUS V_{DD}



VERSUS TEMPERATURE



Vendor: B
P/N:
Rev: (Shrink)
Date Code: 7820

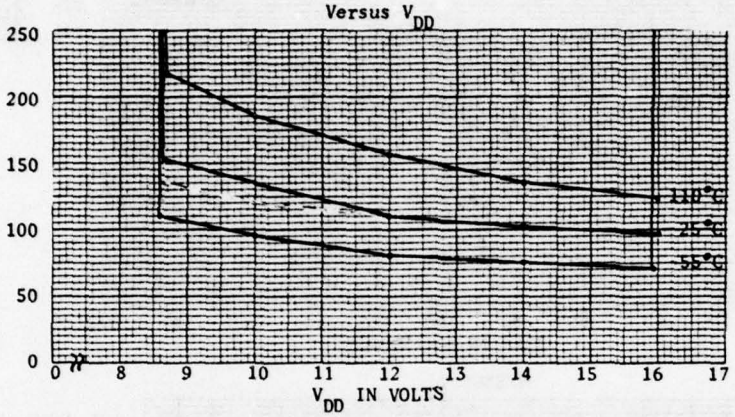
16K DYNAMIC RAM
ACCESS TIME FROM $\overline{RAS}$
t_{RAC}

By J.R.F. 6/12/78

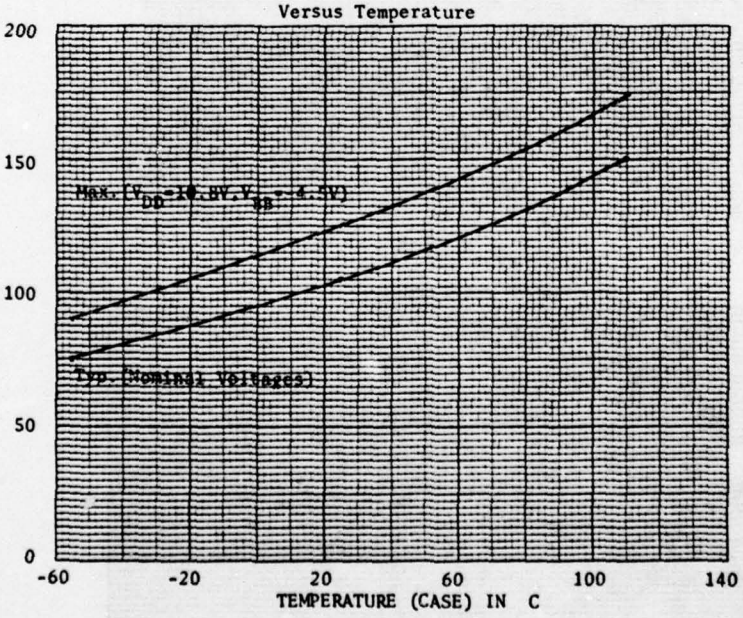
ADDR.PAT = Multiple
DATA PAT = Multiple
LOAD = 1 Schottky TTL
+50pF
V_{BB} = -5.0V
V_{CC} = 5.0V
V_{IHC} = 2.7V
V_{IH} = 2.4V
V_{IL} = 0.8V

W.C. UNIT

Versus V_{DD}



Versus Temperature



Vendor: B
P/N:
REV: (Shrink)
Date Code: 7820
Device: 27

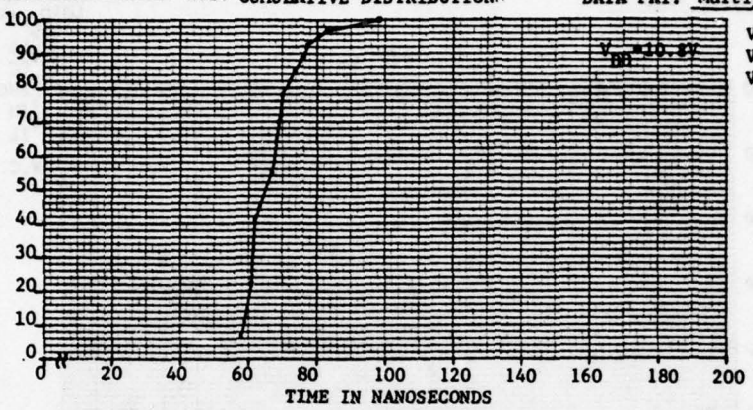
16K DYNAMIC RAM

$\overline{RAS}$ PRECHARGE TIME

t_{RP}

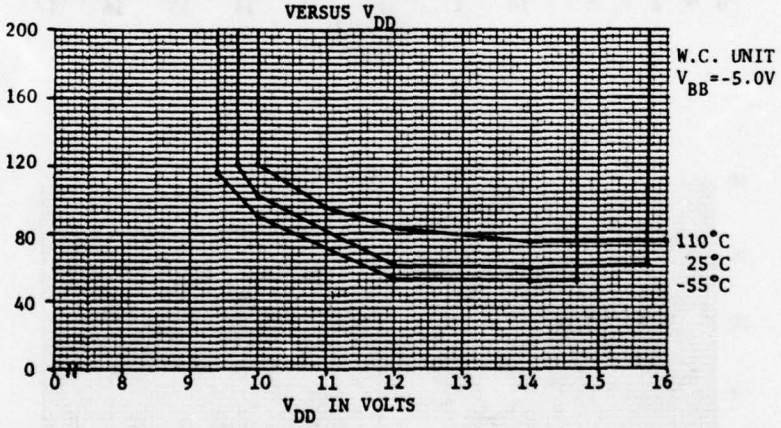
By J.R.F. Date 6/12/78
V_{BB} -4.5V V_{CC} 5.0V
LOAD NA
ADDR PAT. Multiple
DATA PAT. Multiple

W.C. CUMULATIVE DISTRIBUTION

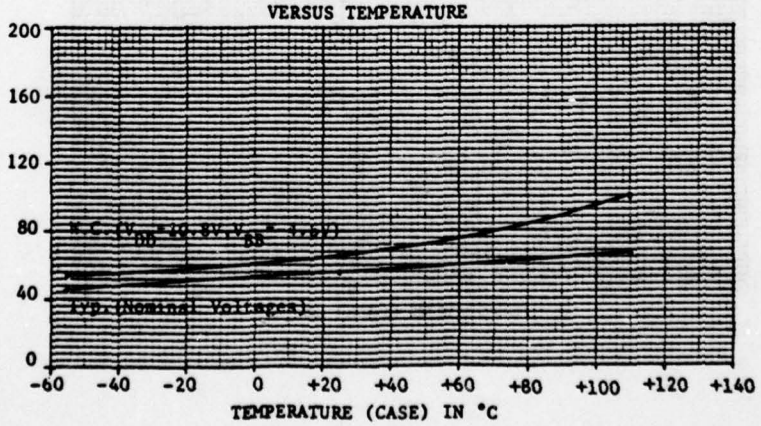


VIHC 2.7V
VIH 2.4V
VIL 0.8V

VERSUS V_{DD}



VERSUS TEMPERATURE



Vendor: B
P/N:
Rev.: (Shrink)
Date Code: 7820

16K DYNAMIC RAM

ROW ADDRESS HOLD TIME

t_{RAH}

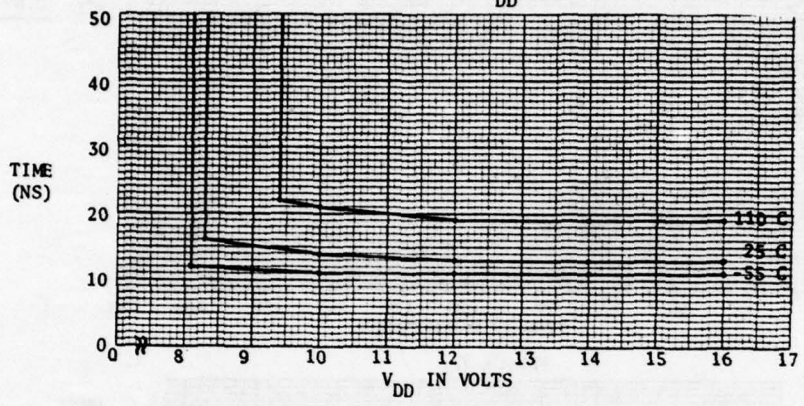
By J.R.F. 6/7/78

ADDR.PAT = Multiple
DATA PAT = Multiple
LOAD =NA

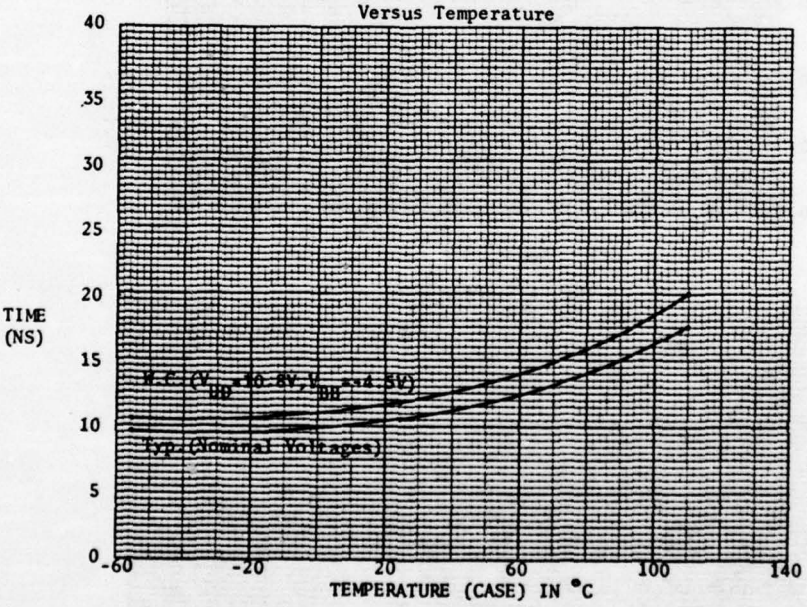
V_{BB} =-5.0V
V_{CC} = 5.0V
V_{IHC} = 2.7V
V_{IH} = 2.4V
V_{IL} = 0.8V

W.C. UNIT

Versus V_{DD}



Versus Temperature



Vendor: B
P/N:
Rev.: (Shrink)
Date Code: 7820

16K DYNAMIC RAM

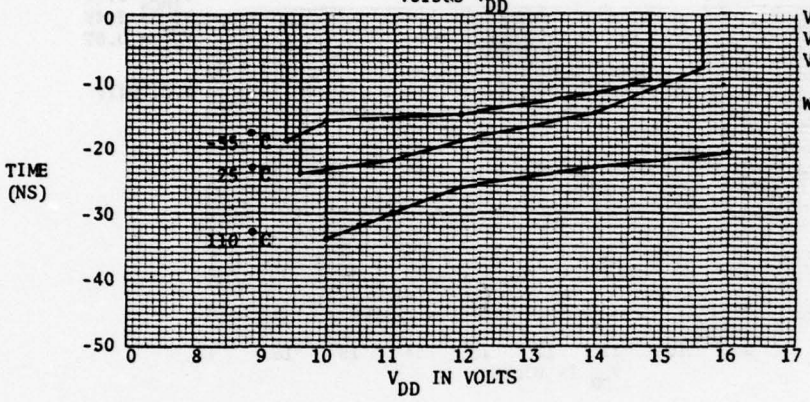
COLUMN ADDRESS SETUP TIME

t_{ASC}

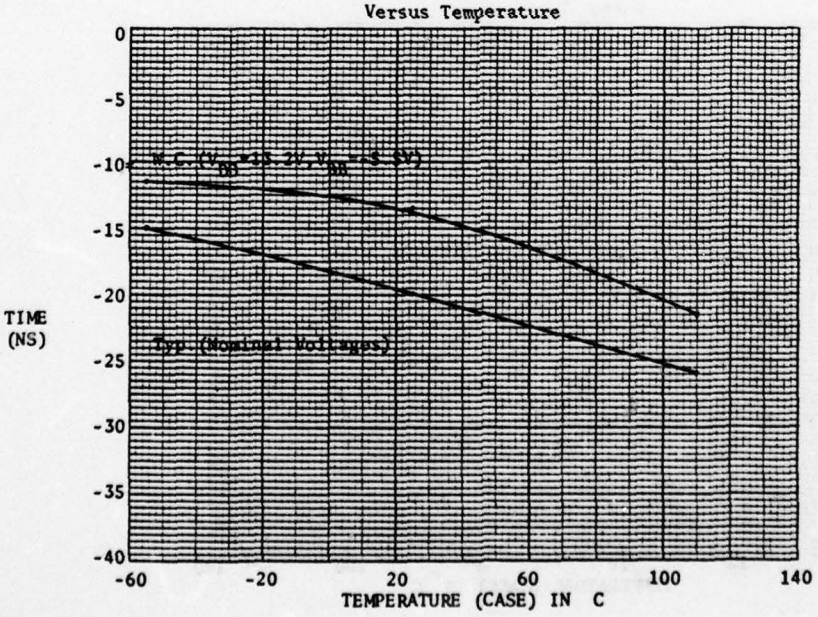
By J.R.F. 6/8/78

ADDR.PAT = Multiple
DATA PAT = Multiple
LOAD = NA
V_{BB} =-5.0V
V_{CC} = 5.0V
V_{IHC} = 2.7V
V_{IH} = 2.4V
V_{IL} = 0.8V
W.C. UNIT

Versus V_{DD}



Versus Temperature



16K DYNAMIC RAM

Vendor: B
P/N:
Rev.: (Shrink)
Date Code: 7820

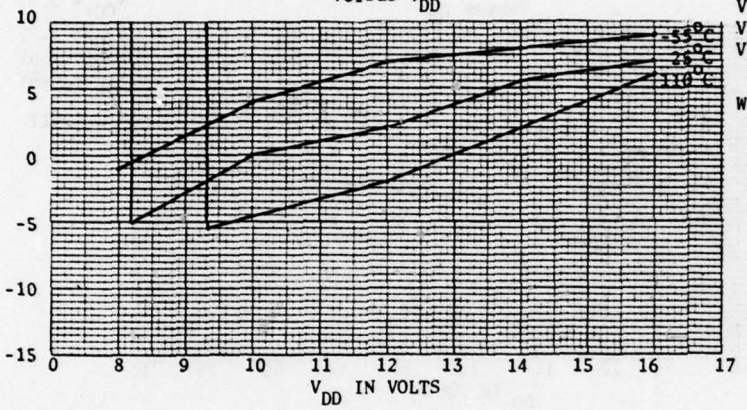
DATA IN SETUP TIME TO $\overline{\text{WRITE}}$

$t_{DS(W)}$

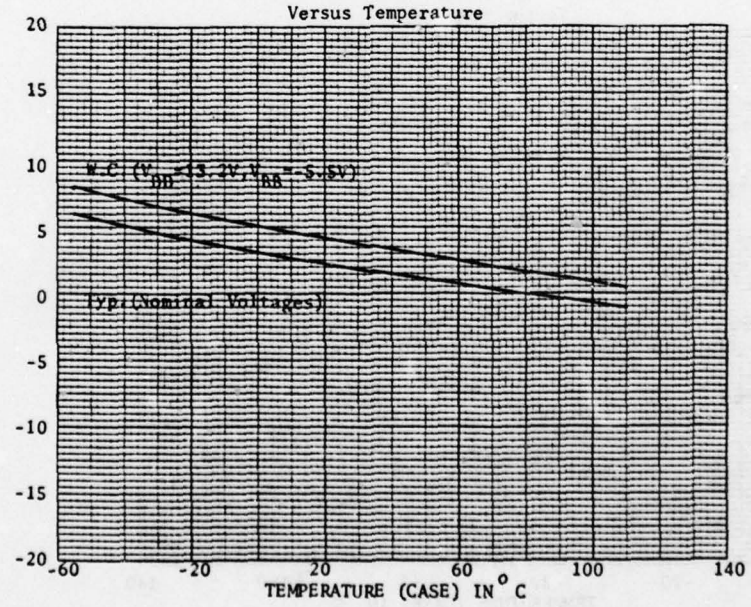
By J.R.F. 6/7/78
ADDR.PAT = Multiple
DATA PAT = Multiple
LOAD = NA
V_{BB} =-5.0V
V_{CC} = 5.0V
V_{IHC} = 2.7V
V_{IH} = 2.4V
V_{IL} = 0.8V

W.C. UNIT

Versus V_{DD}



Versus Temperature



AD-A067 713 IBM FEDERAL SYSTEMS DIV OWEGO N Y F/G 9/2

ELECTRICAL CHARACTERIZATION OF 16K DYNAMIC RAMS.(U)

FEB 79 F D AUSTIN, J R FLORINI, E L HUNTER F30602-77-C-0222

UNCLASSIFIED RADC-TR-79-5 NL

2 OF 2
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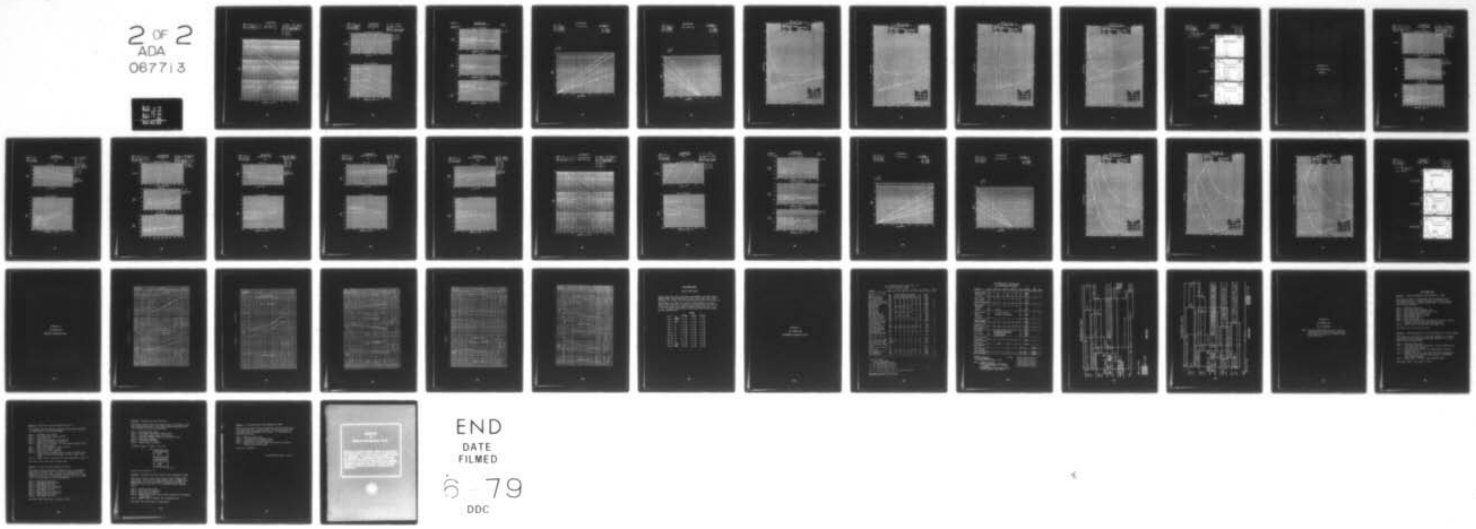
067713



END
DATE
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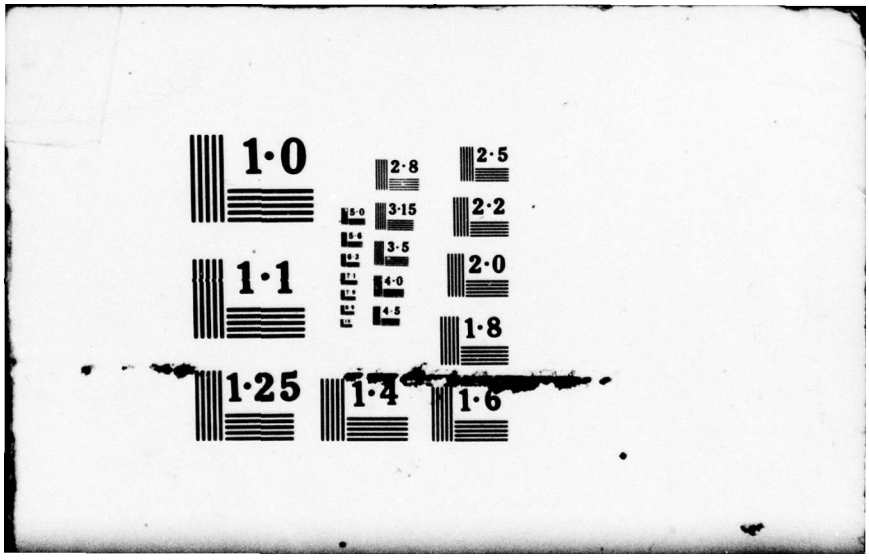
6 79
DDC


1·0
1·1
1·25
1·4
1·6
1·8
2·0
2·2
2·5
2·8
3·15
3·5
4·0
4·5
5·0

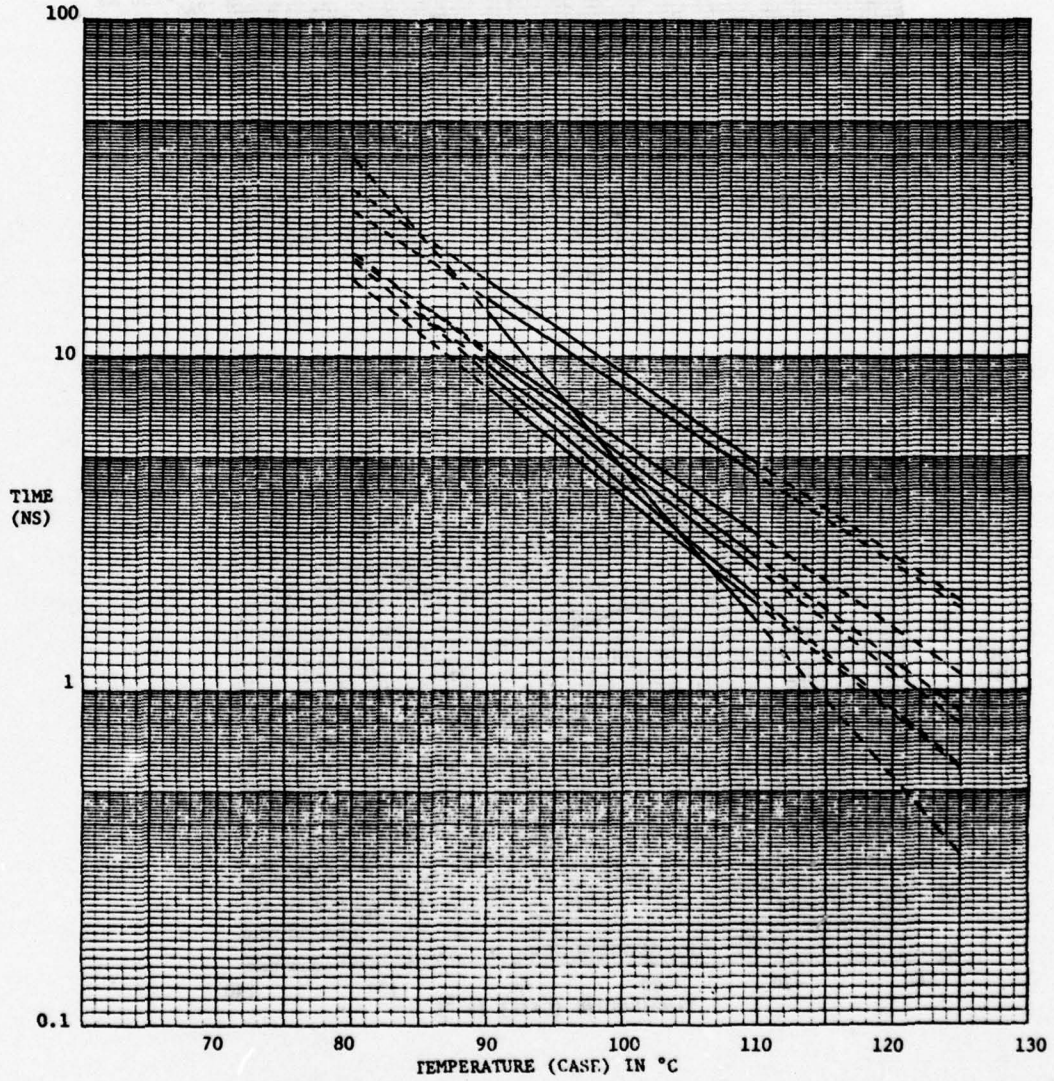
16K DYNAMIC RAM

Vendor: B
P/N:
REV: (Shrink)
Date Code: 7820

CELL RETENTION TIME

REFRESH PERIOD t_{REF}

By E.L.H. Date 7/12/78
V_{DD} 10.8V V_{BB} -5.5V
ADDR. PAT. DYNAMIC REFRESH
DATA PAT. SINGLE X-BAR
V_{IHC} 2.7V
V_{IH} 2.4V
V_{IL} 0.8V



Vendor: B
P/N:
Rev.: (Shrink)
Date Code: 7820
No. Devices: 27

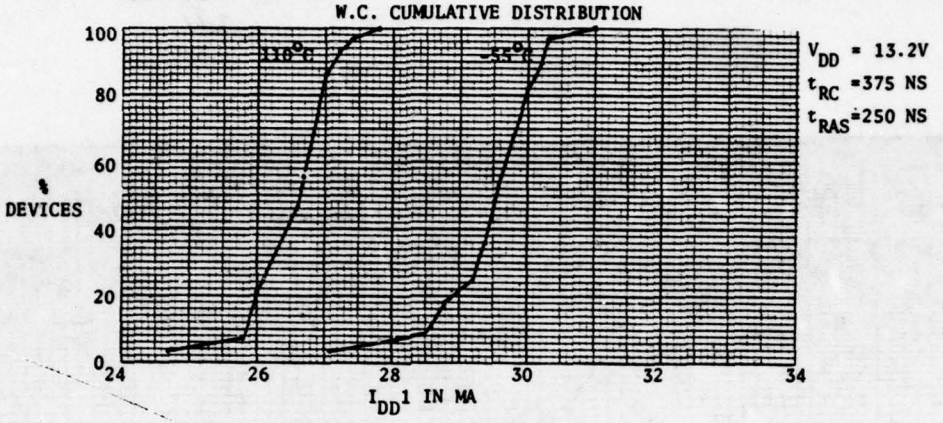
16K DYNAMIC RAM

OPERATING CURRENT
$I_{DD}1$

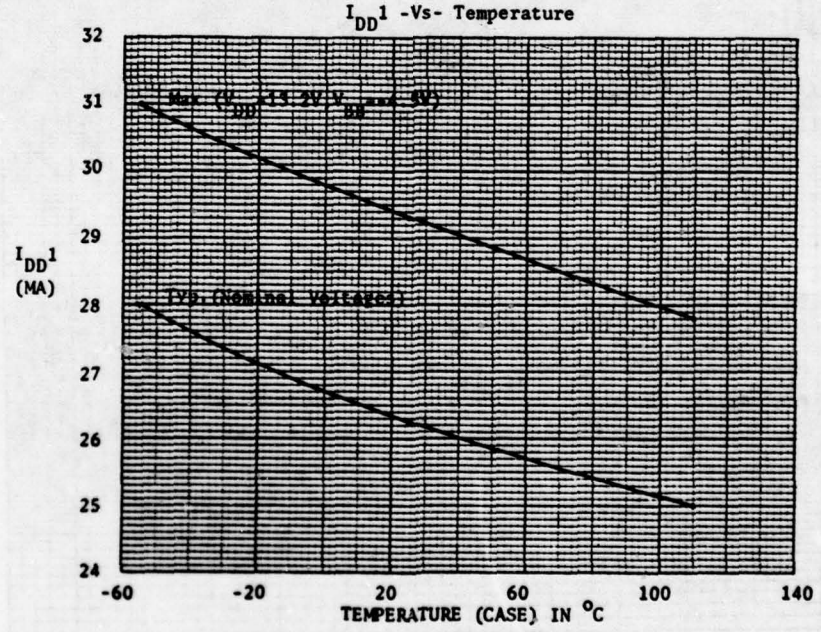
By J.R.F. 5/12/78

V_{BB} = -4.5V V_{CC} = 5.0V
LOAD = NA
ADDR.PAT.= WALKING DIAGONAL
DATA PAT.= MAJOR DIAGONAL

W.C. CUMULATIVE DISTRIBUTION



$I_{DD}1$ -Vs- Temperature



VENDOR B

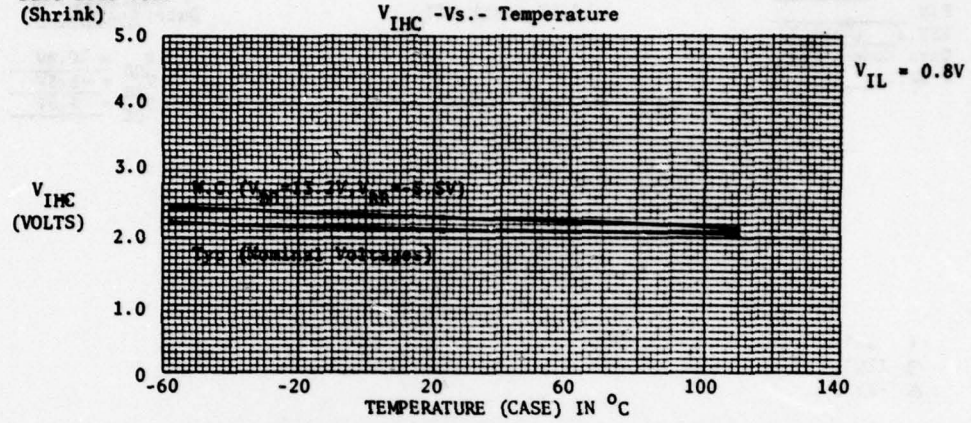
16K DYNAMIC RAM

INPUT LEVEL SENSITIVITY

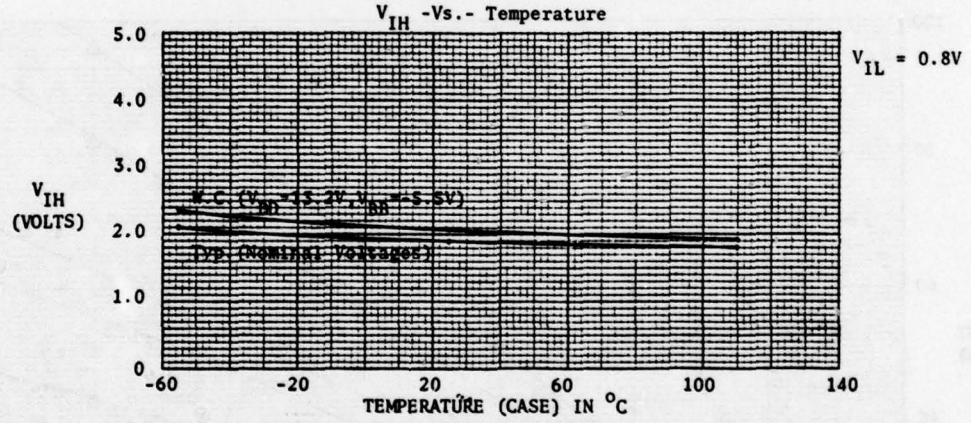
J.R.F.
6/6/78

Date Code 7820
(Shrink)

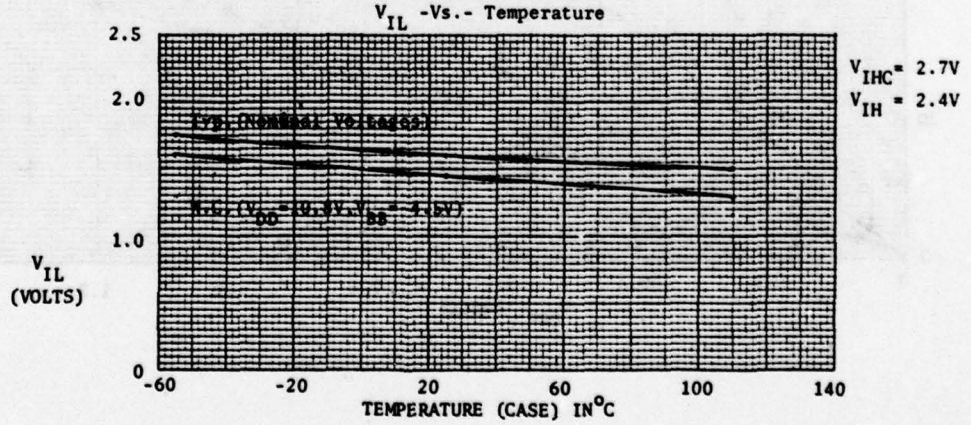
V_{IHC} -Vs.- Temperature



V_{IH} -Vs.- Temperature



V_{IL} -Vs.- Temperature



16K DYNAMIC RAM

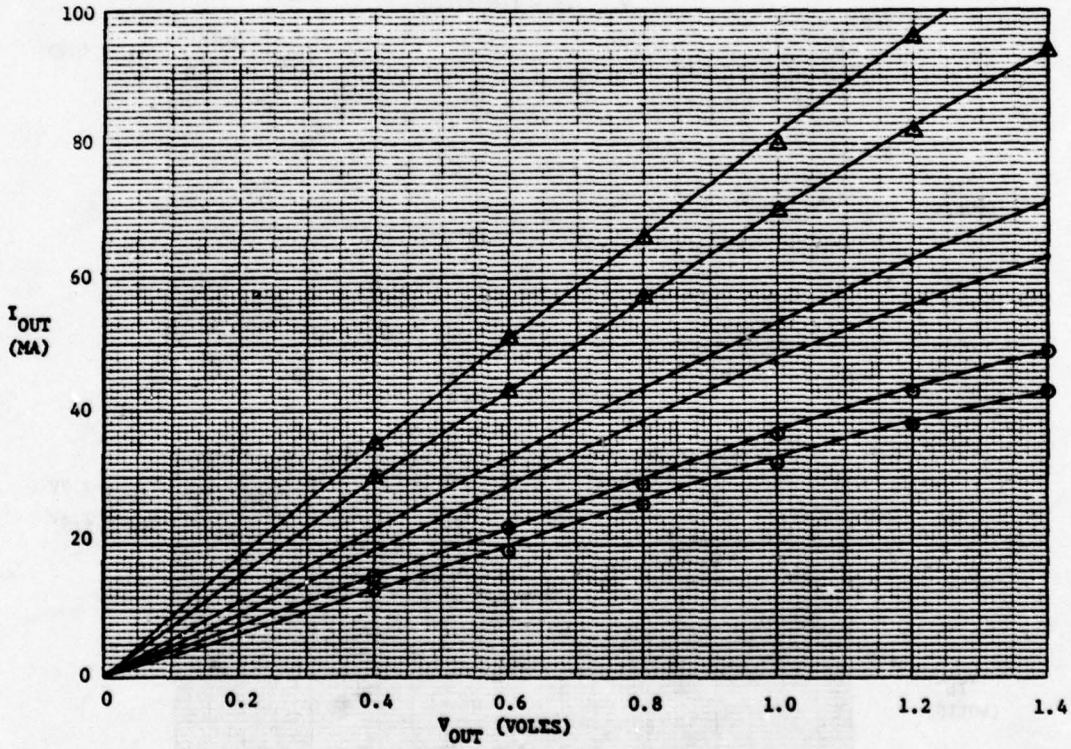
Vendor: B
P/N:
REV.: (Shrink)
Date Code: 7820
DEV.: 7

SINK CURRENT(I_{OL})

By: J.R.F.
Date: 6/29/78

V_{DD} = 10.8V
V_{BB} = -5.5V
V_{CC} = 4.5V

• 25°C
⊙ 110°C
△ -55°C



16K DYNAMIC RAM

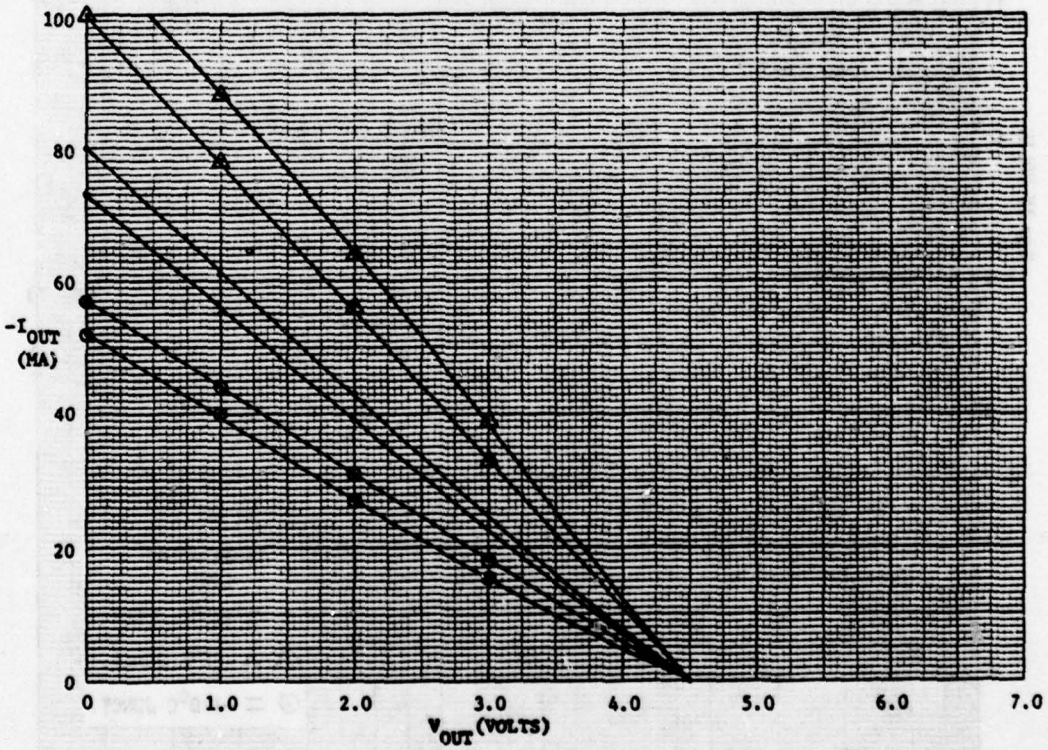
Vendor: B
P/N:
REV.: (Shrink)
Date Code: 7820
DEV.: 7

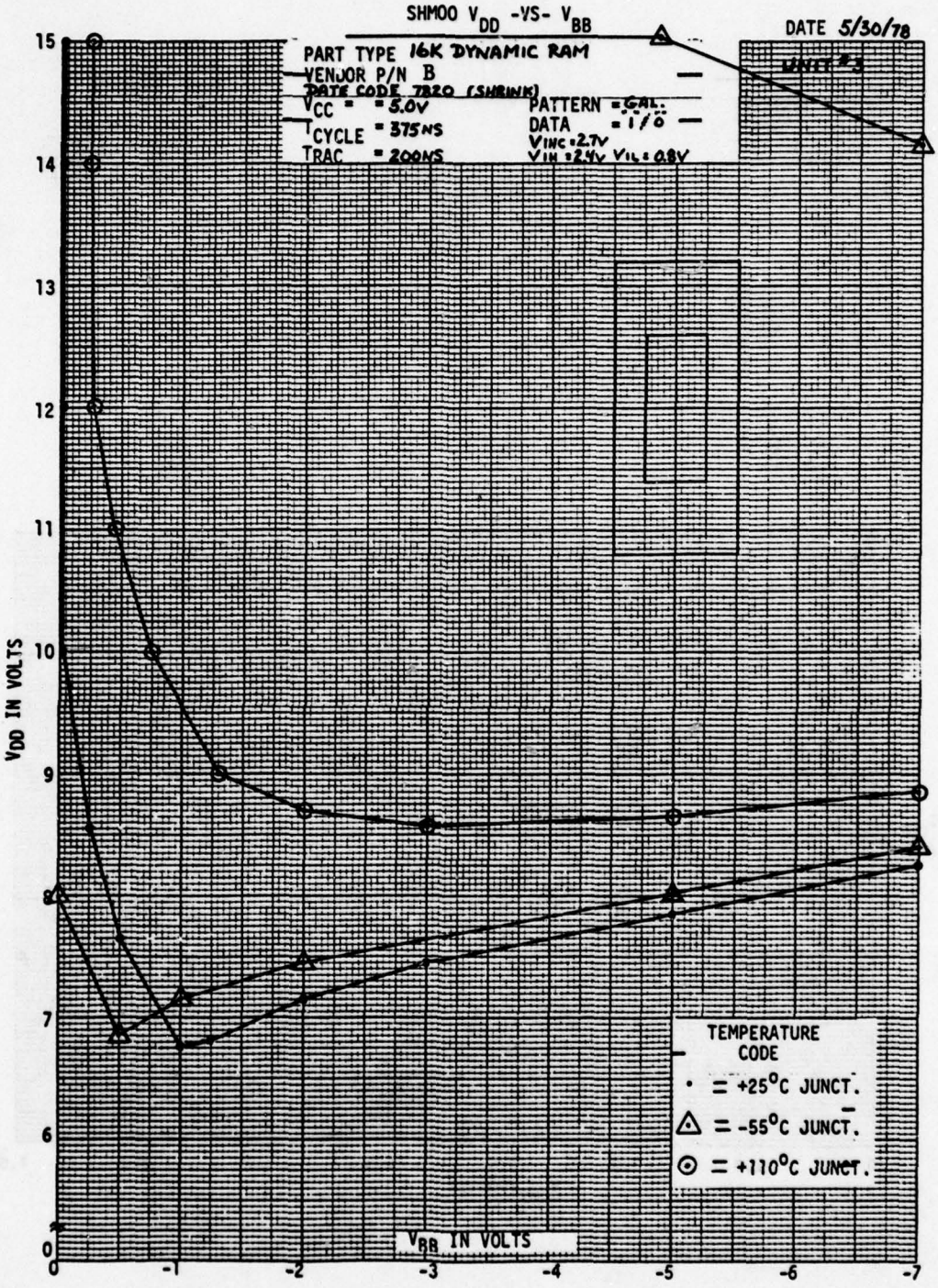
SOURCE CURRENT(I_{OH})

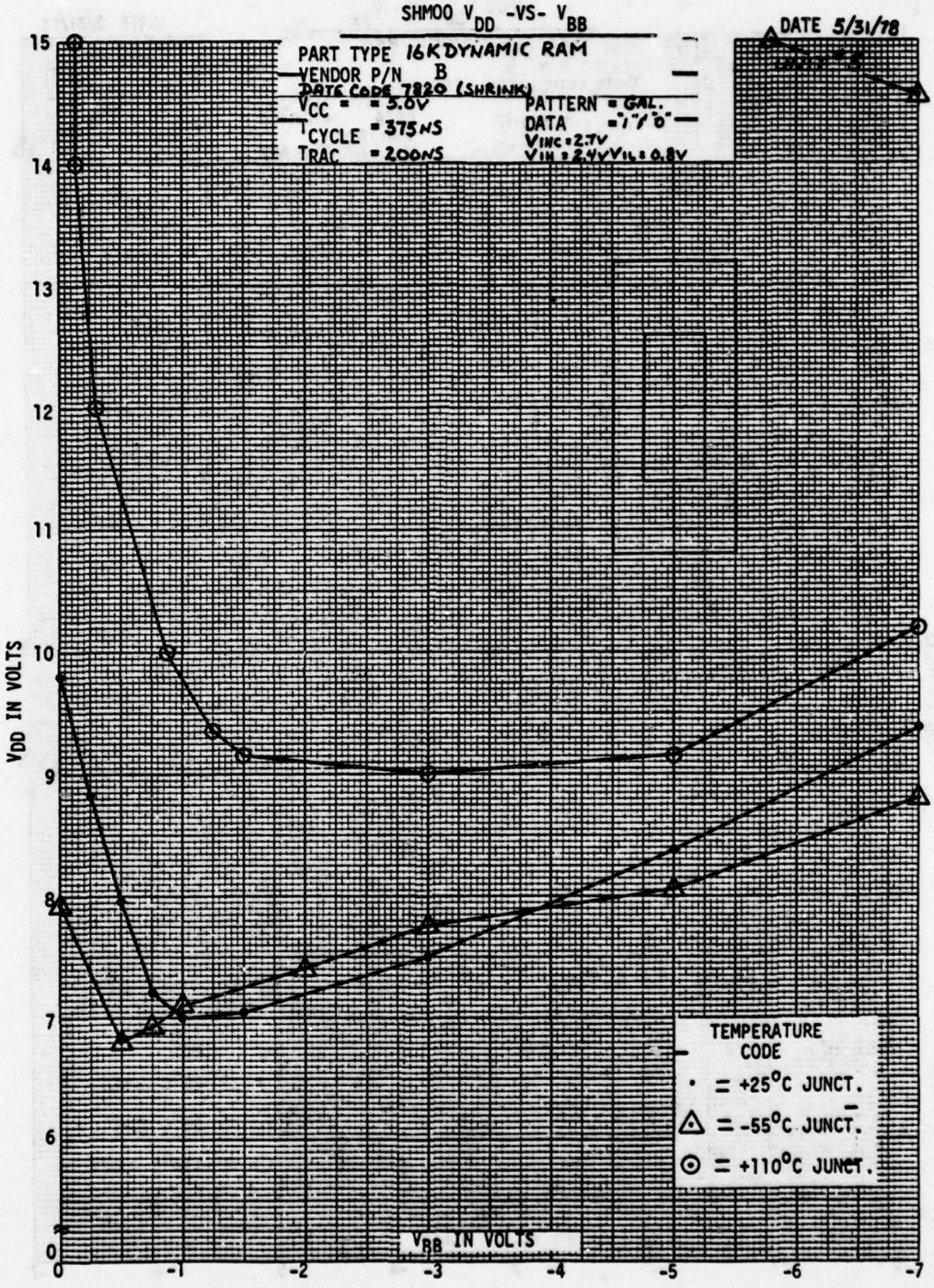
By: J.R.P.
Date: 6/28/78

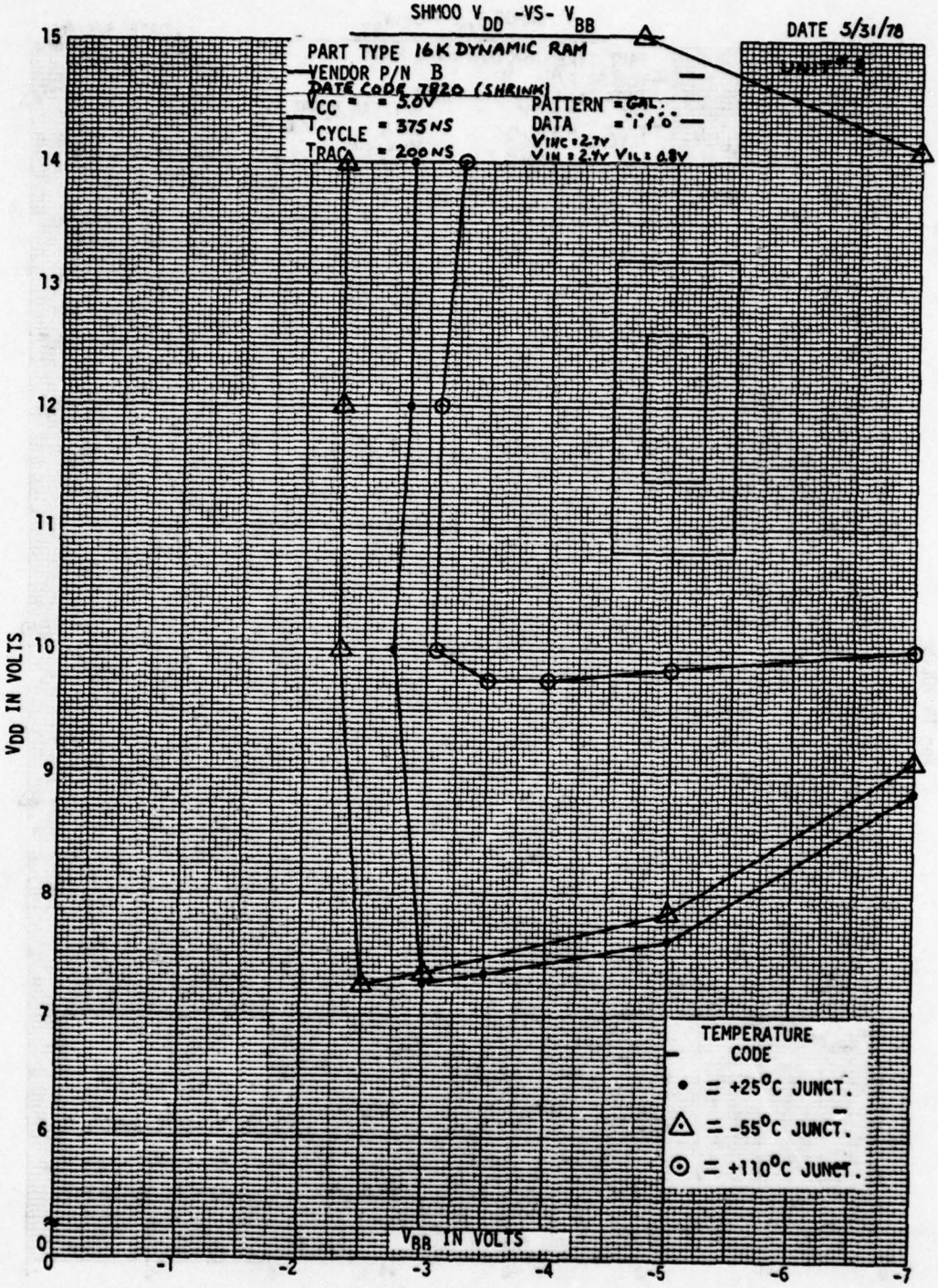
V_{DD} = 10.8V
V_{BB} = -5.5V
V_{CC} = 4.5V

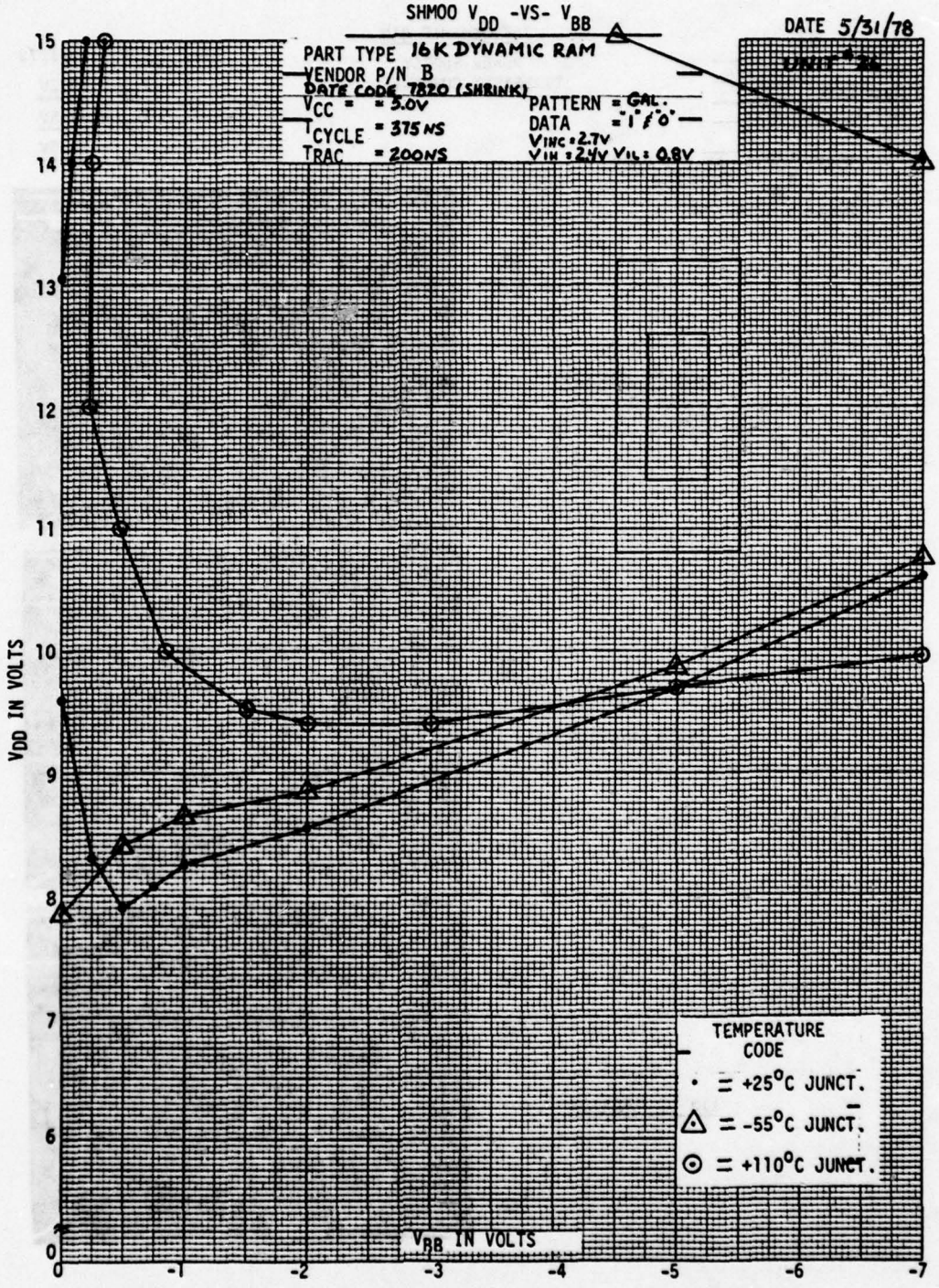
• 25°C
⊙ 110°C
△ -55°C




SHMOO V_{DD} -VS- V_{BB}
DATE 5/30/78
UNIT #3
PART TYPE 16K DYNAMIC RAM
VENJOR P/N B
DATE CODE 7820 (SHRINK)
V_{CC} = 5.0V
T_{CYCLE} = 375NS
T_{RAC} = 200NS
PATTERN = CAL.
DATA = 1/0
V_{INC} = 2.7V
V_{IH} = 2.4V V_{IL} = 0.8V
V_{DD} IN VOLTS
V_{BB} IN VOLTS
TEMPERATURE CODE
• = +25°C JUNCT.
△ = -55°C JUNCT.
⊙ = +110°C JUNCT.


SHMOO V_{DD} -VS- V_{BB}
DATE 5/31/78
PART TYPE 16K DYNAMIC RAM
VENDOR P/N B
DATE CODE 7820 (SHRINK)
V_{CC} = 5.0V
T_{CYCLE} = 375NS
T_{RAC} = 200NS
PATTERN = GAL.
DATA = "1'S 0"
V_{INC} = 2.7V
V_{IH} = 2.4V V_{IL} = 0.8V
V_{DD} IN VOLTS
V_{BB} IN VOLTS
TEMPERATURE CODE
• = +25°C JUNCT.
△ = -55°C JUNCT.
⊙ = +110°C JUNCT.


SHM00 V_{DD} -VS- V_{BB}
DATE 5/31/78
PART TYPE 16K DYNAMIC RAM
VENDOR P/N B
DATE CODE 7820 (SHRINK)
V_{CC} = 5.0V
T_{CYCLE} = 375 NS
T_{RAC} = 200 NS
PATTERN = GAL.
DATA = 1 1 0
V_{IHC} = 2.7V
V_{IH} = 2.4V V_{IL} = 0.8V
V_{DD} IN VOLTS
V_{BB} IN VOLTS
TEMPERATURE CODE
• = +25°C JUNCT.
△ = -55°C JUNCT.
⊙ = +110°C JUNCT.


SHMOO V_{DD} -VS- V_{BB}
DATE 5/31/78
PART TYPE 16K DYNAMIC RAM
VENDOR P/N B
DATE CODE 7820 (SHRINK)
V_{CC} = = 5.0V
T_{CYCLE} = 375 NS
T_{RAC} = 200NS
PATTERN = GAL.
DATA = 1's 0's
V_{INC} = 2.7V
V_{IH} = 2.4V V_{IL} = 0.8V
V_{DD} IN VOLTS
V_{BB} IN VOLTS
TEMPERATURE CODE
• = +25°C JUNCT.
△ = -55°C JUNCT.
⊙ = +110°C JUNCT.

VENDOR: B
P/N:
Date Code: 7820
Rev.: (SHRINK)

16K DYNAMIC RAM

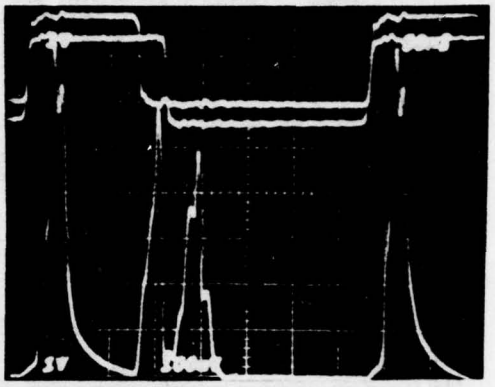
POWER SUPPLY
TRANSIENT CURRENTS

By: J.R.F. 6/1/78

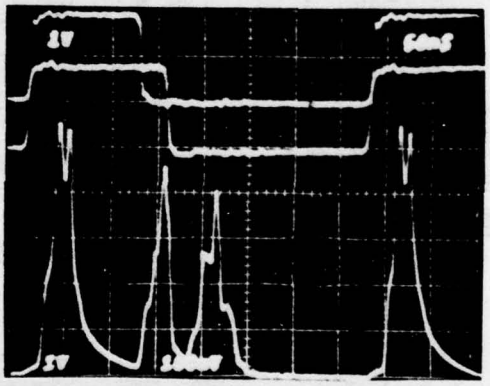
V_{DD} = 13.2V
V_{BB} = -4.5V
V_{CC} = 5.0V

Vert.: $\overline{RAS}$ & $\overline{CAS}$ = 1 V/CM
I_{DD} = 20 MA/CM
Horiz.: 50 NS/CM

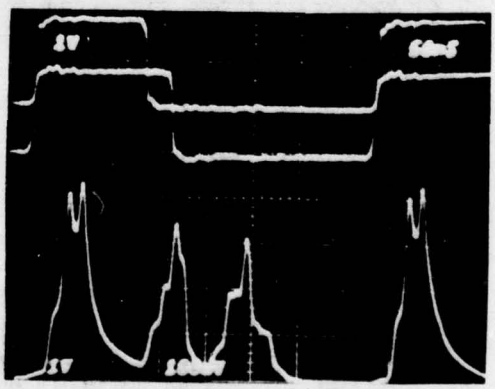
-55 °C JUNCTION



25 °C JUNCTION



110 °C JUNCTION



APPENDIX III

16K DYNAMIC RAM

VENDOR C

Vendor: C
P/N:
REV:
Date Code: 0278
Device: 25

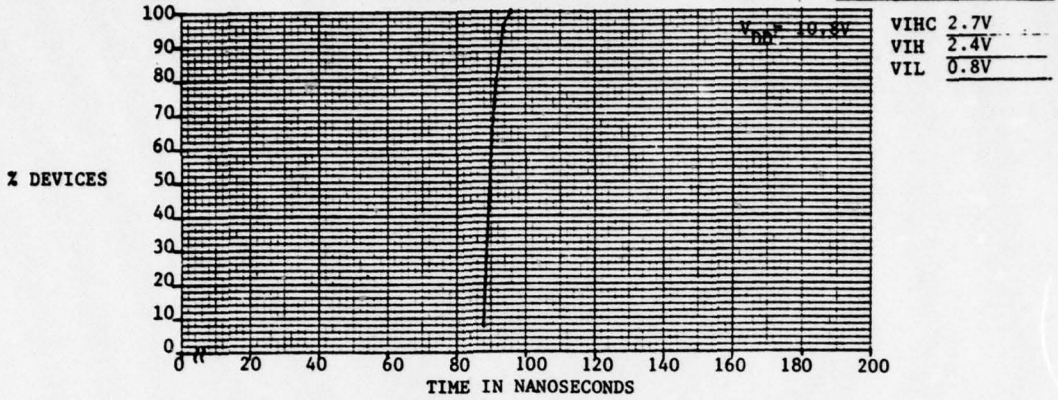
16K DYNAMIC RAM

ACCESS TIME FROM $\overline{CAS}$

t_{CAC}

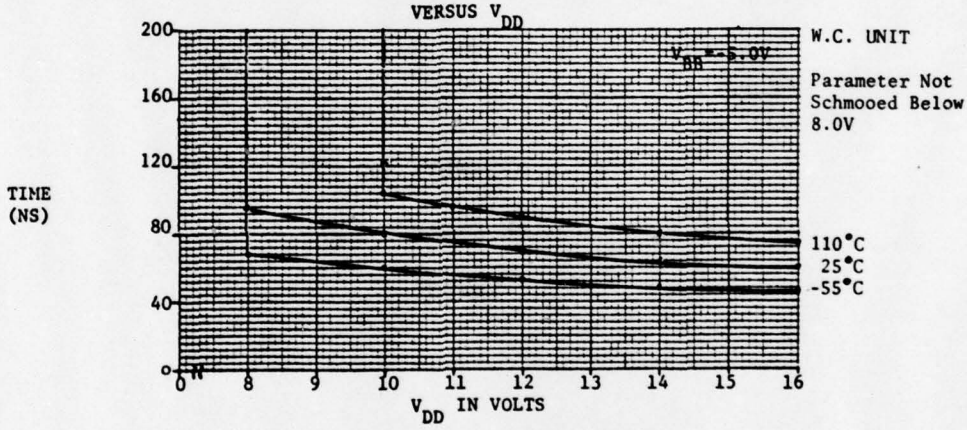
W.C. CUMULATIVE DISTRIBUTION

By J.R.F. Date 6/8/78
V_{BB} -4.5V V_{CC} 5.0V
LOAD 1 Schottky TTL + 50pF
ADDR PAT. Multiple
DATA PAT. Multiple



VIHC 2.7V
VIH 2.4V
VIL 0.8V

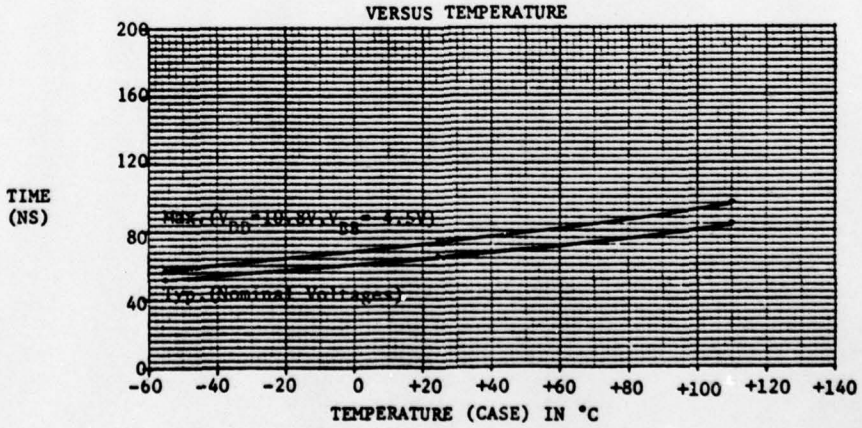
VERSUS V_{DD}



W.C. UNIT

Parameter Not Schmooed Below 8.0V

VERSUS TEMPERATURE



Vendor: C
P/N:
Rev:
Date Code: 0278

16K DYNAMIC RAM

ACCESS TIME FROM $\overline{RAS}$

t_{RAC}

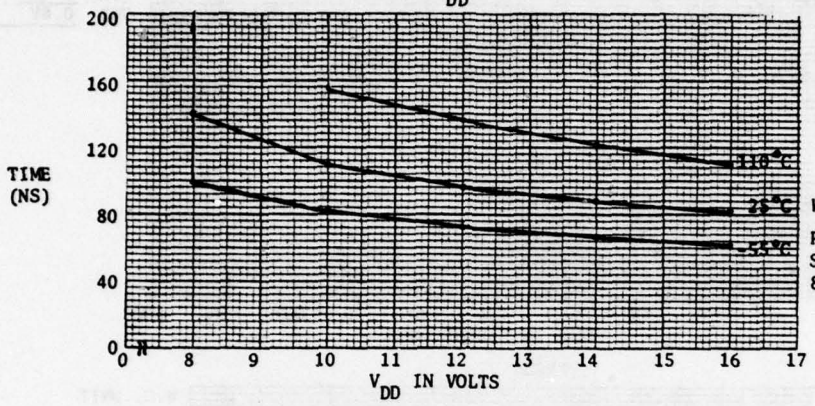
By J.R.F Date 6/8/78

V_{BB} = -5.0V
V_{CC} = 5.0V
LOAD= 1 Schottky TTL + 50pF
ADDR.PAT = Multiple
DATA PAT = Multiple
V_{IHC} = 2.7V
V_{IH} = 2.4V
V_{IL} = 0.8V

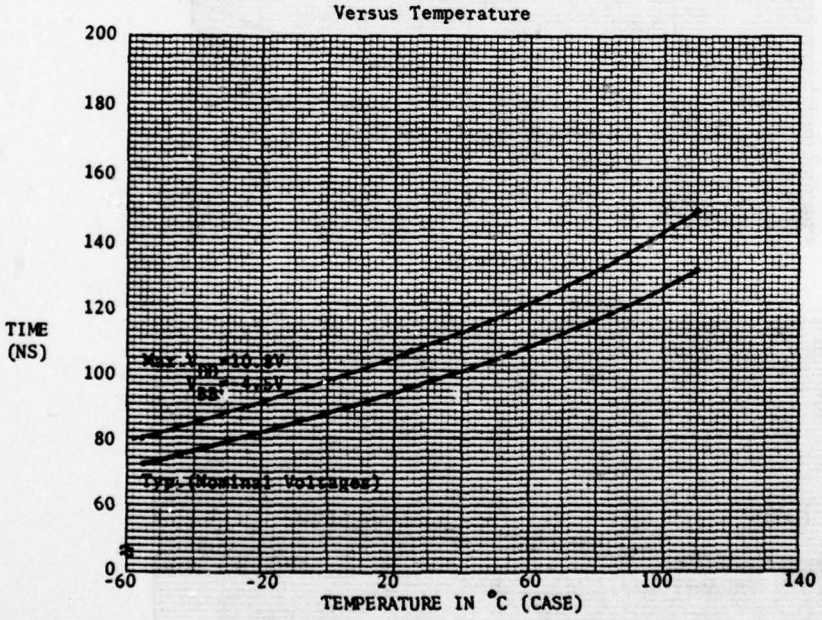
W.C. UNIT

Parameter Not Schmooed Below 8.0V

Versus V_{DD}



Versus Temperature



Vendor: C
P/N:
REV:
Date Code: 0278
Device: 25

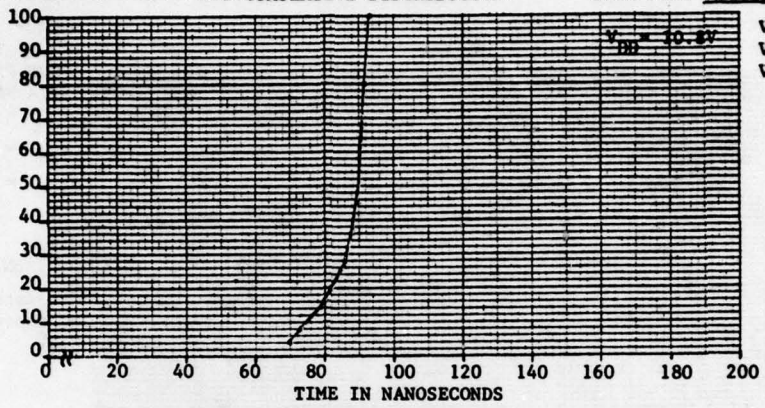
16K DYNAMIC RAM

$\overline{RAS}$ PRECHARGE TIME

t_{RP}

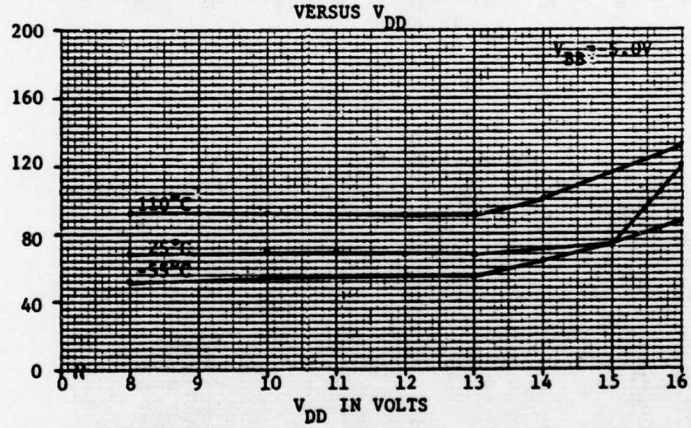
By J.R.F. Date 5/25/78
V_{BB} -4.5V V_{CC} 5.0V
LOAD NA
ADDR PAT. Multiple
DATA PAT. Multiple

W.C. CUMULATIVE DISTRIBUTION:



VIHC 2.7V
VIH 2.4V
VIL 0.8V

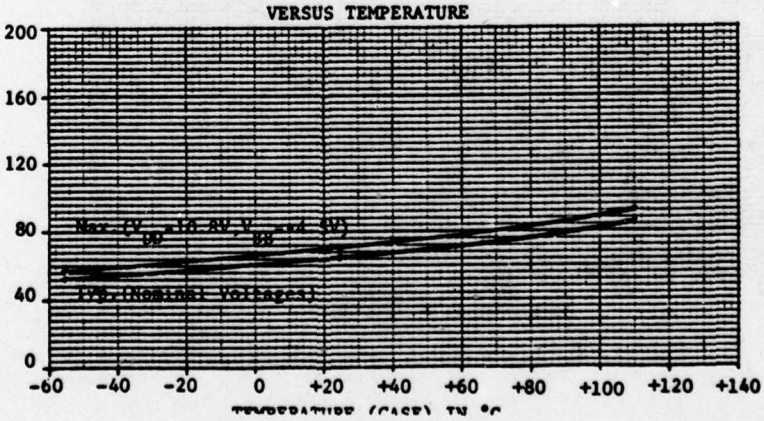
VERSUS V_{DD}



W.C. UNIT

Parameter Not Schmooed Below 8.0V

VERSUS TEMPERATURE



Vendor: C
P/N:
Rev.:
Date Code: 0278

16K DYNAMIC RAM

ROW ADDRESS HOLD TIME

t_{RAH}

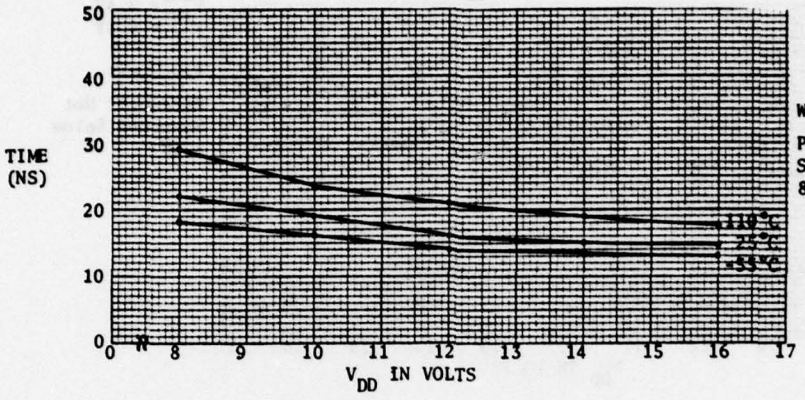
By J.R.F. Date 6/8/78

ADDR.PAT = Multiple
DATA PAT = Multiple
LOAD = NA
V_{BB} = -5.0V
V_{CC} = 5.0V
V_{IHC} = 2.7V
V_{IH} = 2.4V
V_{IL} = 0.8V

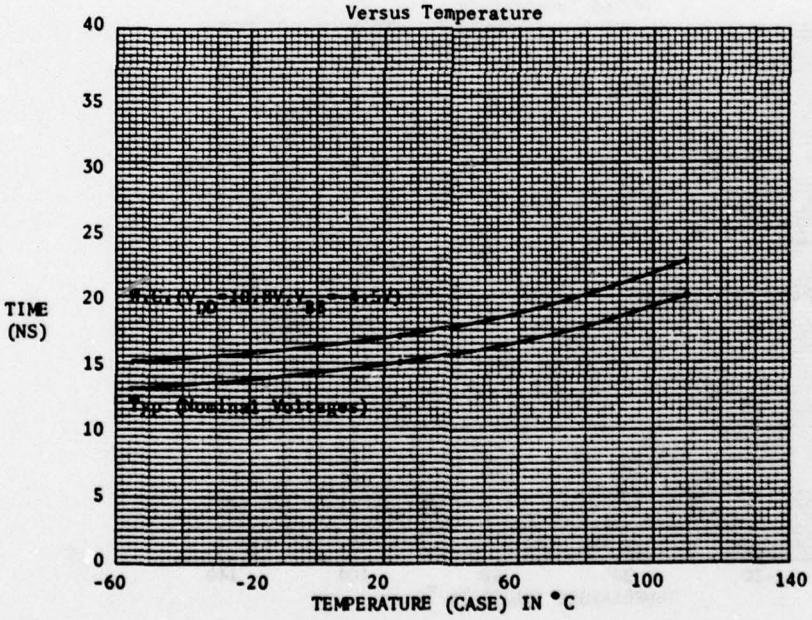
W.C. UNIT

Parameter Not Schmooed Below 8.0V

Versus V_{DD}



Versus Temperature



Vendor: C
P/N:
Rev.:
Date Code: 0278

16K DYNAMIC RAM

COLUMN ADDRESS SETUP TIME

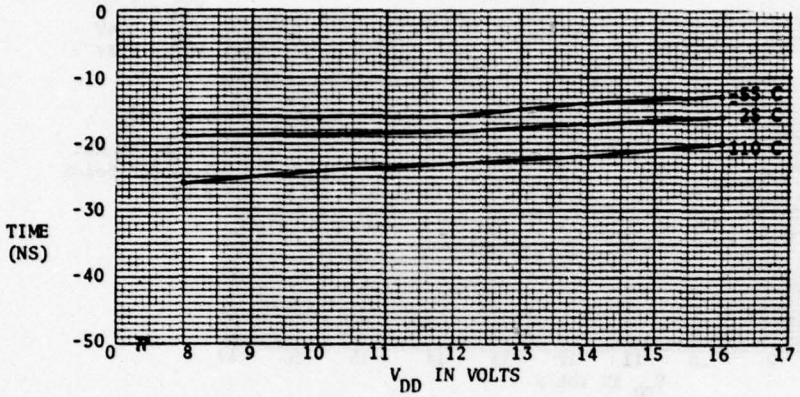
t_{ASC}

By J.R.F. 6/8/78
ADDR.PAT = Multiple
DATA PAT = Multiple
LOAD = NA
V_{BB} = -5.0V
V_{CC} = 5.0V
V_{IHC} = 2.7V
V_{IH} = 2.4V
V_{IL} = 0.8V

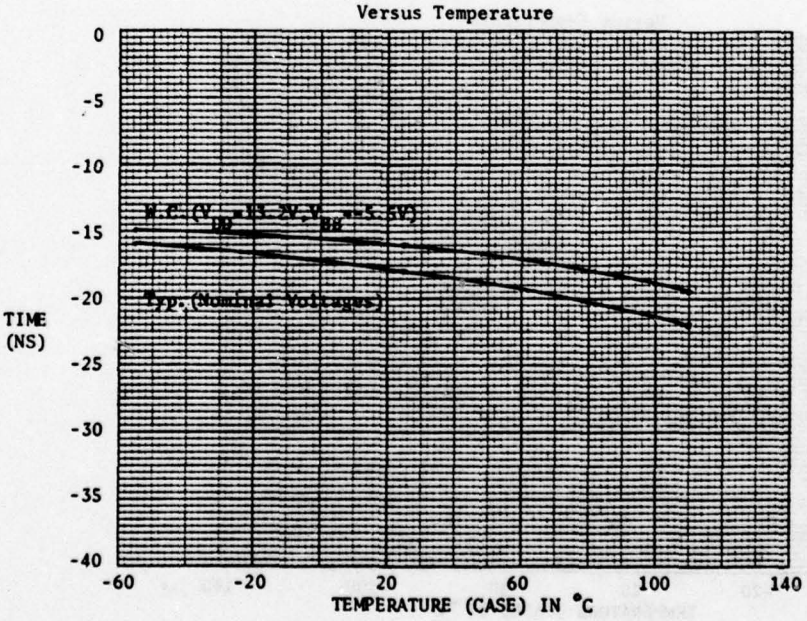
W.C. unit

Parameter Not Schmooed Below 8.0V

Versus V_{DD}



Versus Temperature



Vendor: C
P/N:
Rev.:
Date Code: 0278

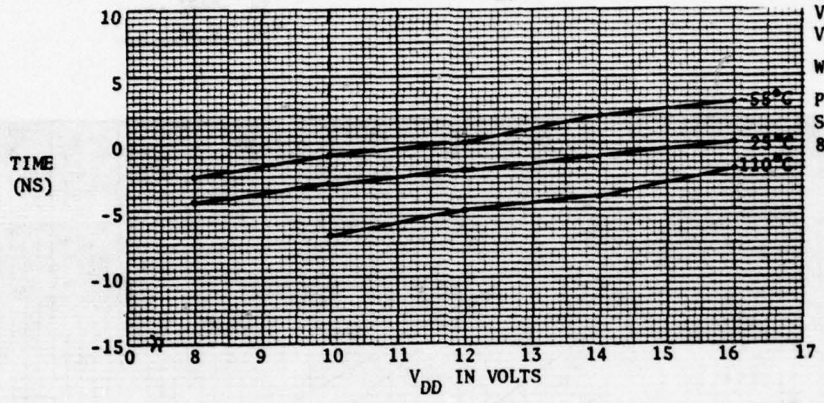
16K DYNAMIC RAM

DATA IN SETUP TIME TO WRITE

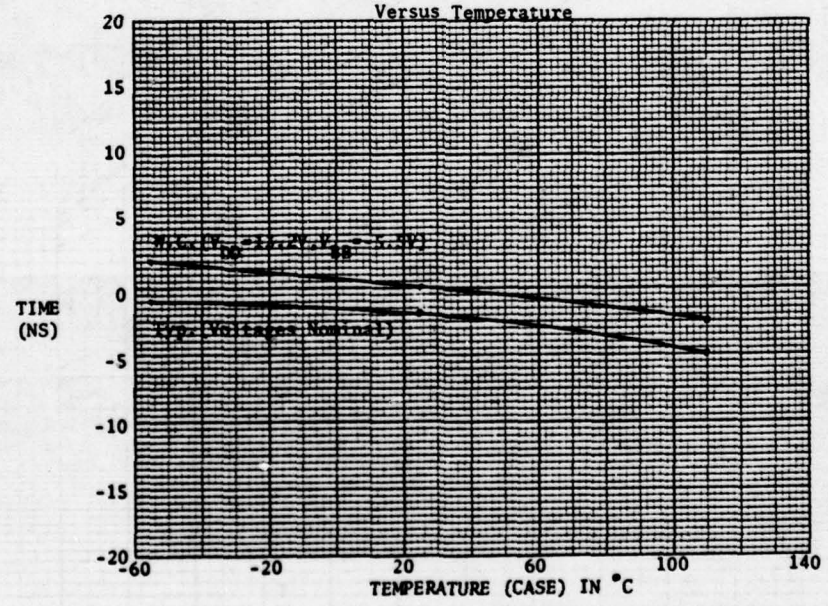
$t_{DS(W)}$

By J.R.F. 6/8/78
ADDR.PAT = Multiple
DATA PAT = Multiple
LOAD = NA
V_{BB} = -5.0V
V_{CC} = 5.0V
V_{IHC} = 2.4V
V_{IH} = 0.8V
V_{IL} = 0.8V
W.C. UNIT
Parameter Not Schmooed Below 8.0V

Versus V_{DD}



Versus Temperature

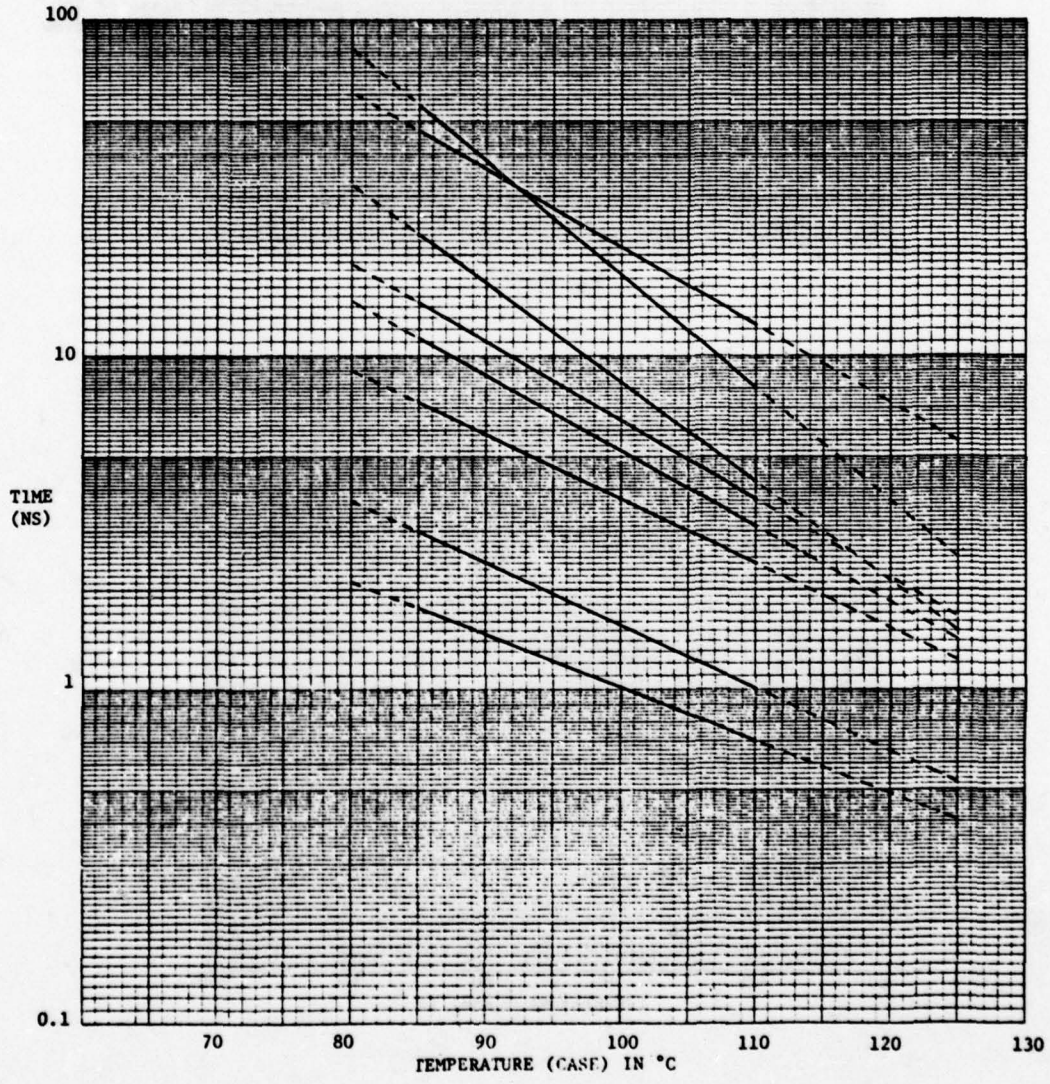


16K DYNAMIC RAM

Vendor: C
P/N:
REV:
Date Code: 0278

CELL RETENTION TIME
REFRESH PERIOD t_{REF}

By E.L.H. Date 7/12/78
V_{DD} 10.8V V_{BB} -5.5V
ADDR. PAT. DYNAMIC REFRESH
DATA PAT. SINGLE X-BAR
V_{IHC} 2.7V
V_{IH} 2.4V
V_{IL} 0.8V



Vendor: C
P/N:
Rev.:
Date Code: 0278
No. Devices: 25

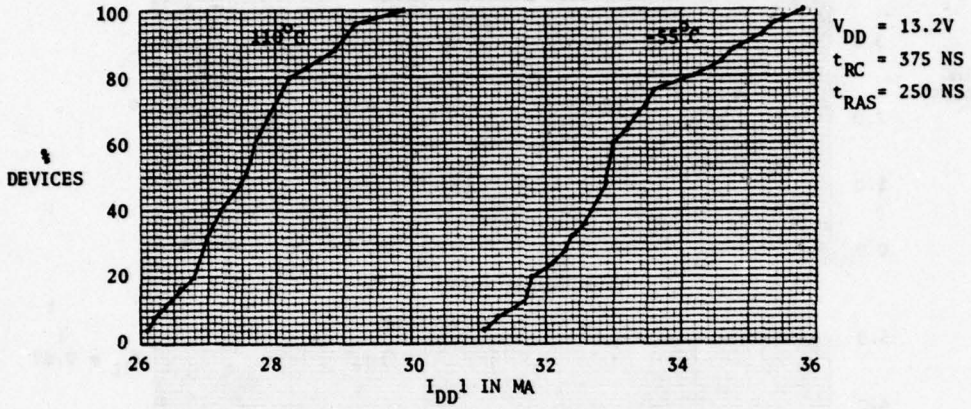
16K DYNAMIC RAM

OPERATING CURRENT
$I_{DD}1$

By J.R.F. 5/17/78

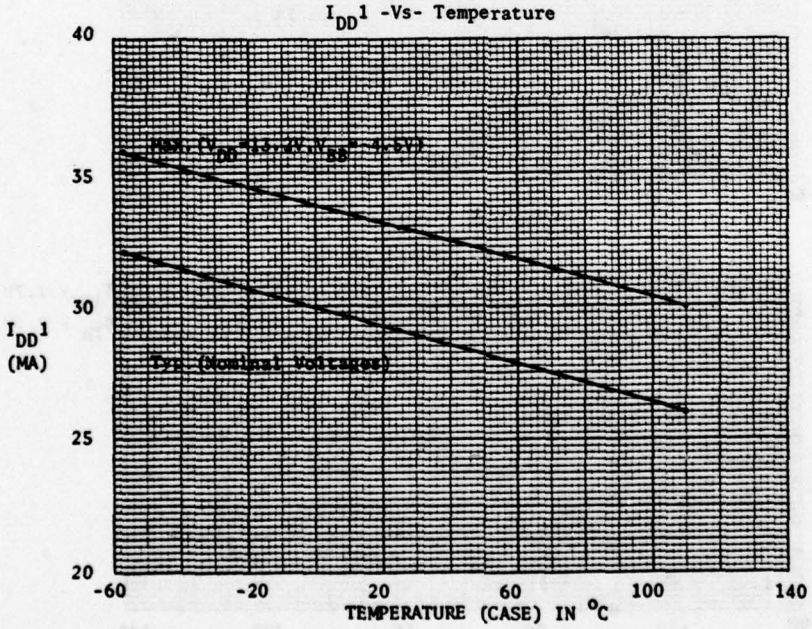
V_{BB} = -4.5V V_{CC} = 5.0V
LOAD = NA
ADDR.PAT.=WALKING DIAGONAL
DATA PAT.=MAJOR DIAGONAL

W.C. CUMULATIVE DISTRIBUTION



V_{DD} = 13.2V
t_{RC} = 375 NS
t_{RAS} = 250 NS

$I_{DD}1$ -Vs- Temperature



16K DYNAMIC RAM

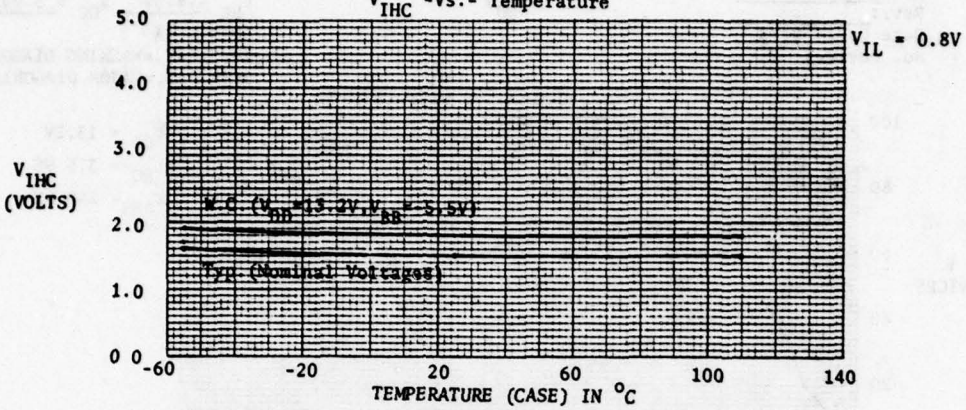
VENDOR C

INPUT LEVEL SENSITIVITY

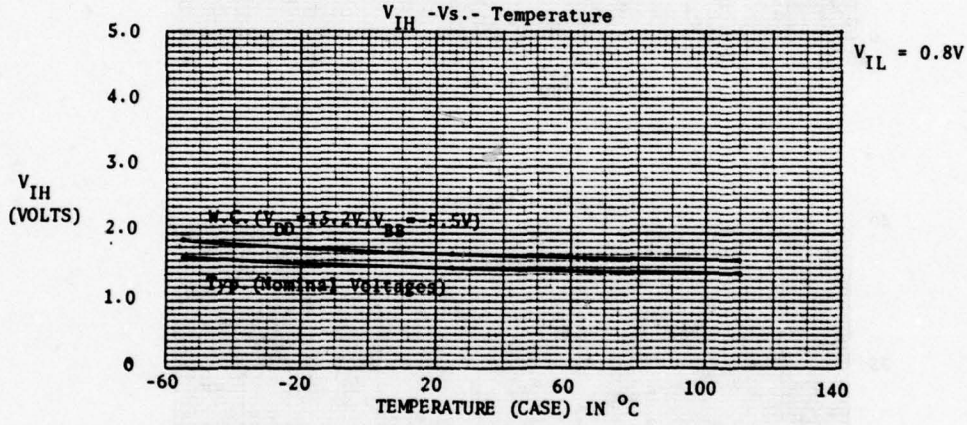
J.R.F.
6/19/78

Date Code 0278

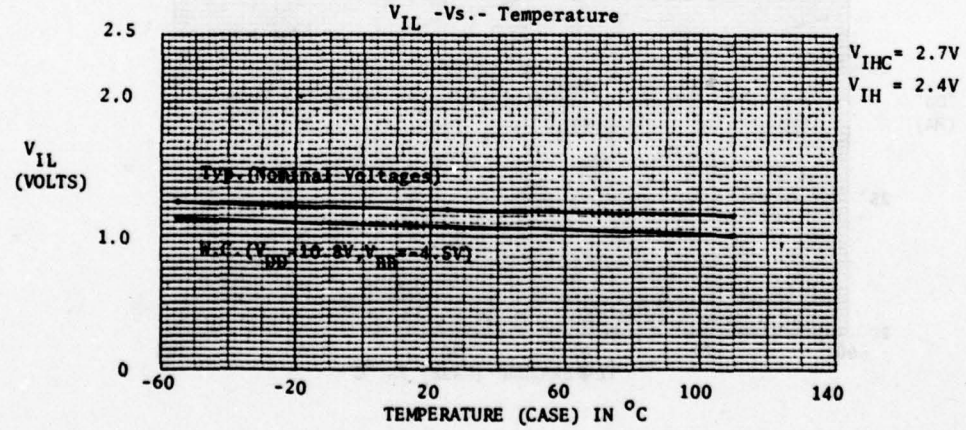
V_{IHC} -Vs.- Temperature



V_{IH} -Vs.- Temperature



V_{IL} -Vs.- Temperature



16K DYNAMIC RAM

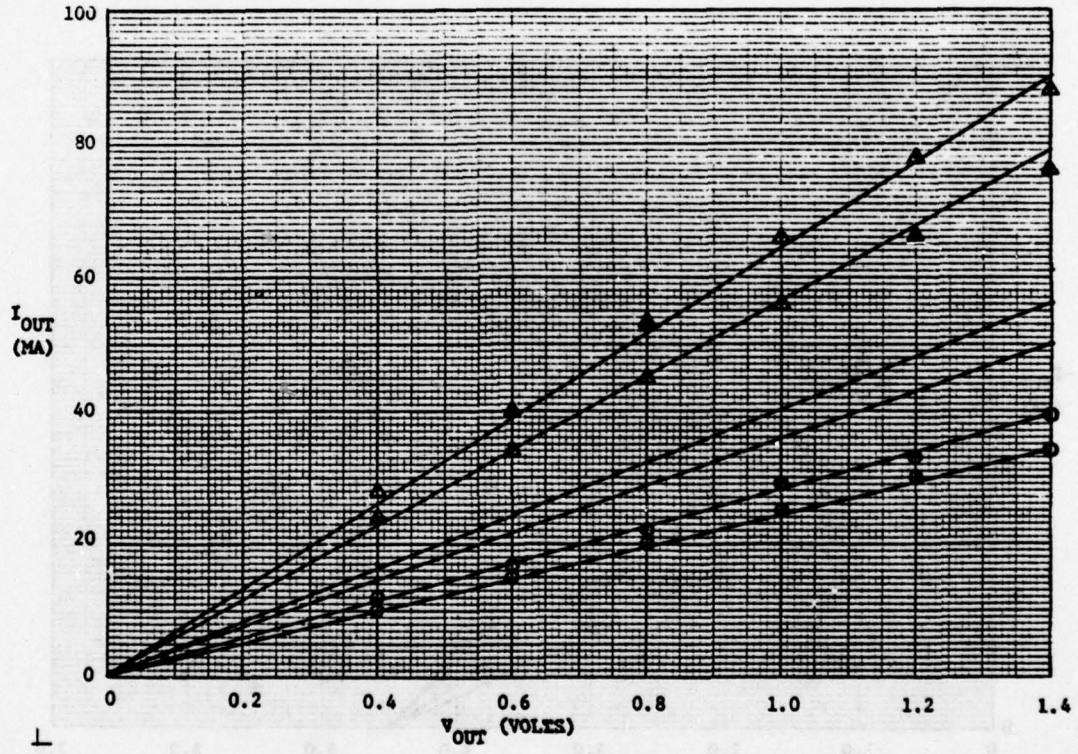
Vendor: C
P/N:
REV.:
Date Code: 0278
DEV.: 7

SINK CURRENT(I_{OL})

By: J.R.F.
Date: 6/29/78

V_{DD} = 10.8V
V_{BB} = -5.5V
V_{CC} = 4.5V

• 25°C
⊙ 110°C
△ -55°C



16K DYNAMIC RAM

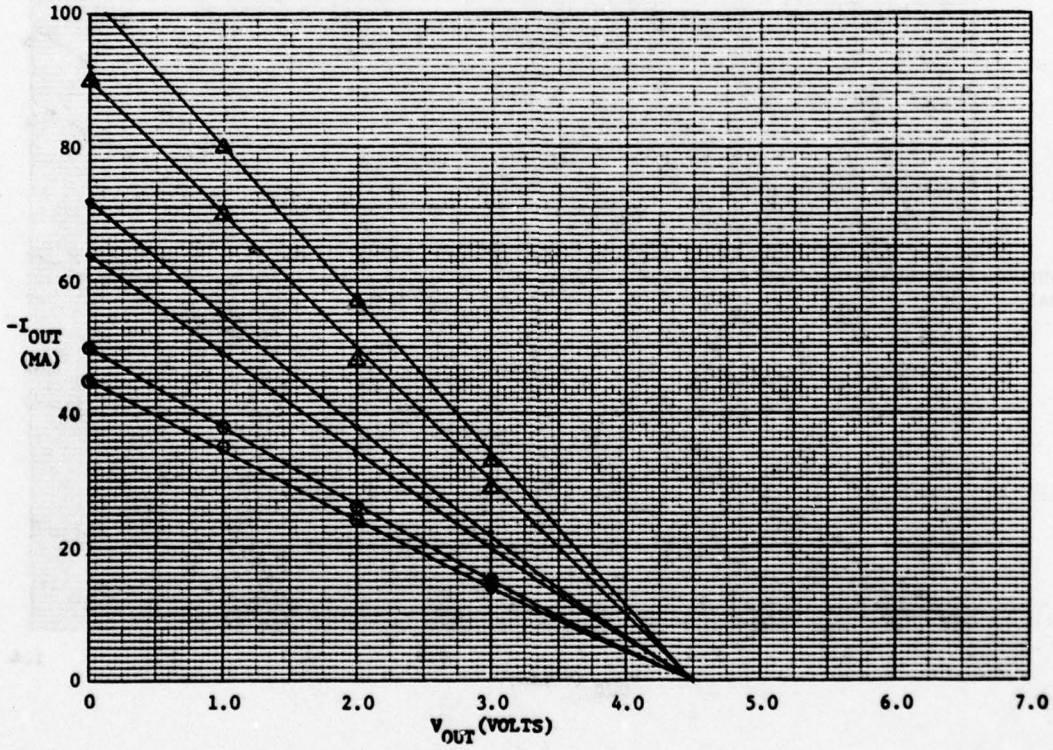
Vendor: C
P/N:
REV.:
Date Code: 0278
DEV.: 7

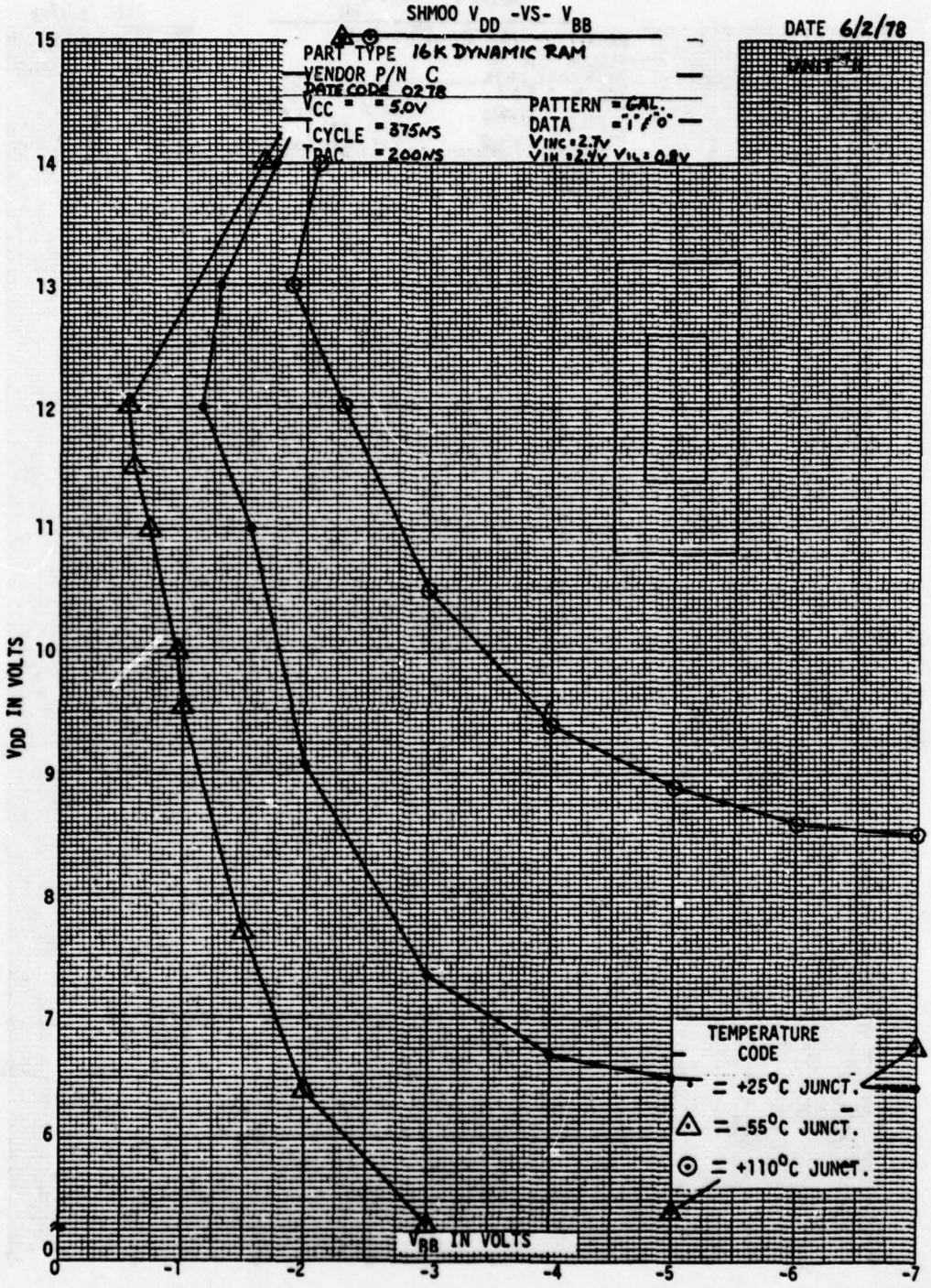
SOURCE CURRENT(I_{OH})

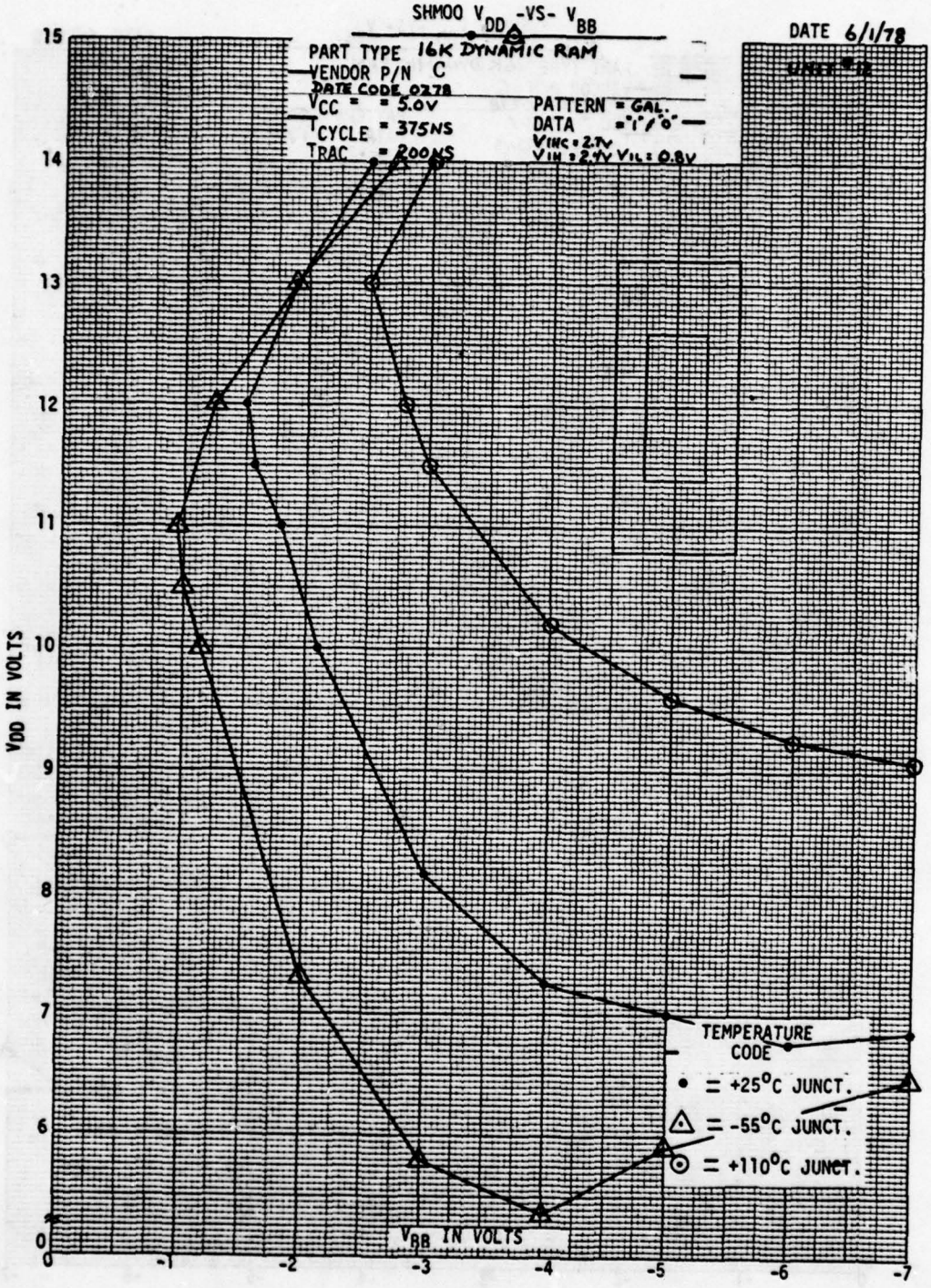
By: J.R.F.
Date: 6/28/78

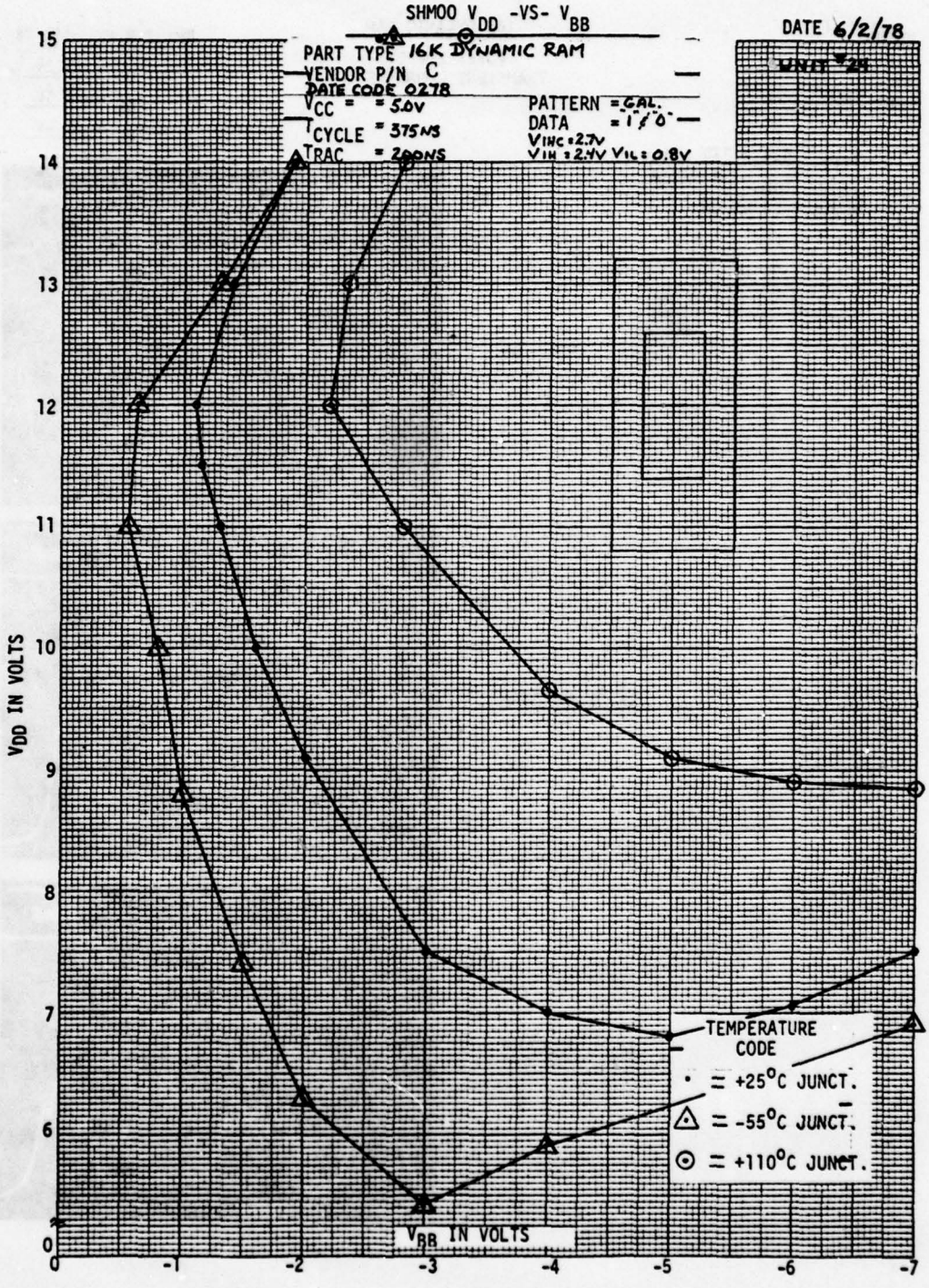
V_{DD} = 10.8V
V_{BB} = -5.5V
V_{CC} = 4.5V

• 25°C
⊙ 110°C
△ -55°C




SHMOO V_{DD} -VS- V_{BB}
DATE 6/2/78
PART TYPE 16K DYNAMIC RAM
VENDOR P/N C
DATE CODE 0278
V_{CC} = 5.0V
T_{CYCLE} = 375NS
T_{RAC} = 200NS
PATTERN = CAL.
DATA = "1" / "0"
V_{INC} = 2.7V
V_{IH} = 2.4V V_{IL} = 0.8V
V_{DD} IN VOLTS
V_{BB} IN VOLTS
15
14
13
12
11
10
9
8
7
6
0
-1
-2
-3
-4
-5
-6
-7
TEMPERATURE CODE
= +25°C JUNCT.
= -55°C JUNCT.
= +110°C JUNCT.


SHMOO V_{DD} -VS- V_{BB}
DATE 6/1/78
PART TYPE 16K DYNAMIC RAM
VENDOR P/N C
DATE CODE 0278
V_{CC} = 5.0V
T_{CYCLE} = 375NS
T_{RAC} = 200NS
PATTERN = GAL.
DATA = "1"/"0"
V_{IHC} = 2.7V
V_{IH} = 2.4V V_{IL} = 0.8V
V_{DD} IN VOLTS
V_{BB} IN VOLTS
TEMPERATURE CODE
• = +25°C JUNCT.
△ = -55°C JUNCT.
⊙ = +110°C JUNCT.


SHMOO V_{DD} -VS- V_{BB}
DATE 6/2/78
PART TYPE 16K DYNAMIC RAM
VENDOR P/N C
DATE CODE 0278
UNIT #24
V_{CC} = 5.0V
T_{CYCLE} = 375NS
T_{RAC} = 200NS
PATTERN = GAL.
DATA = 1 / 0
V_{INC} = 2.7V
V_{IH} = 2.4V V_{IL} = 0.8V
V_{DD} IN VOLTS
V_{BB} IN VOLTS
TEMPERATURE CODE
• = +25°C JUNCT.
△ = -55°C JUNCT.
⊙ = +110°C JUNCT.
15
14
13
12
11
10
9
8
7
6
0
-1
-2
-3
-4
-5
-6
-7

VENDOR: C
P/N:
Rev.:
Date Code: 0278

16K DYNAMIC RAM

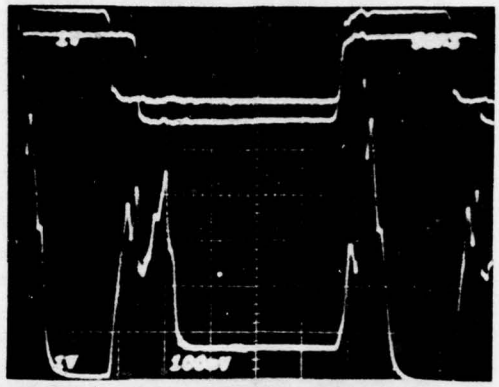
POWER SUPPLY
TRANSIENT CURRENTS

By: J.R.F. 6/2/78

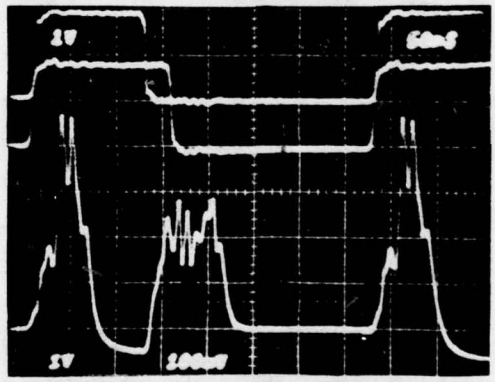
V_{DD} = 13.2V
V_{BB} = -4.5V
V_{CC} = 5.0V

Vert.: $\overline{RAS}$ & $\overline{CAS}$ = 1 V/CM
I_{DD} = 20 MA/CM
Horiz.: 50 NS/CM

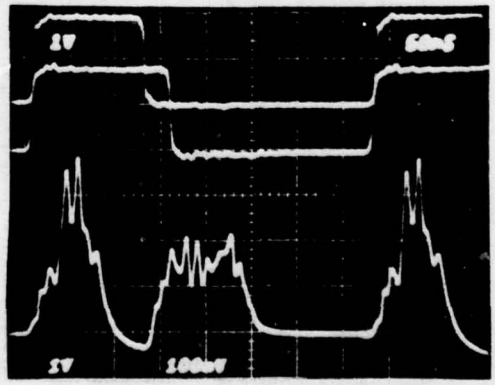
-55 °C JUNCTION



25 °C JUNCTION



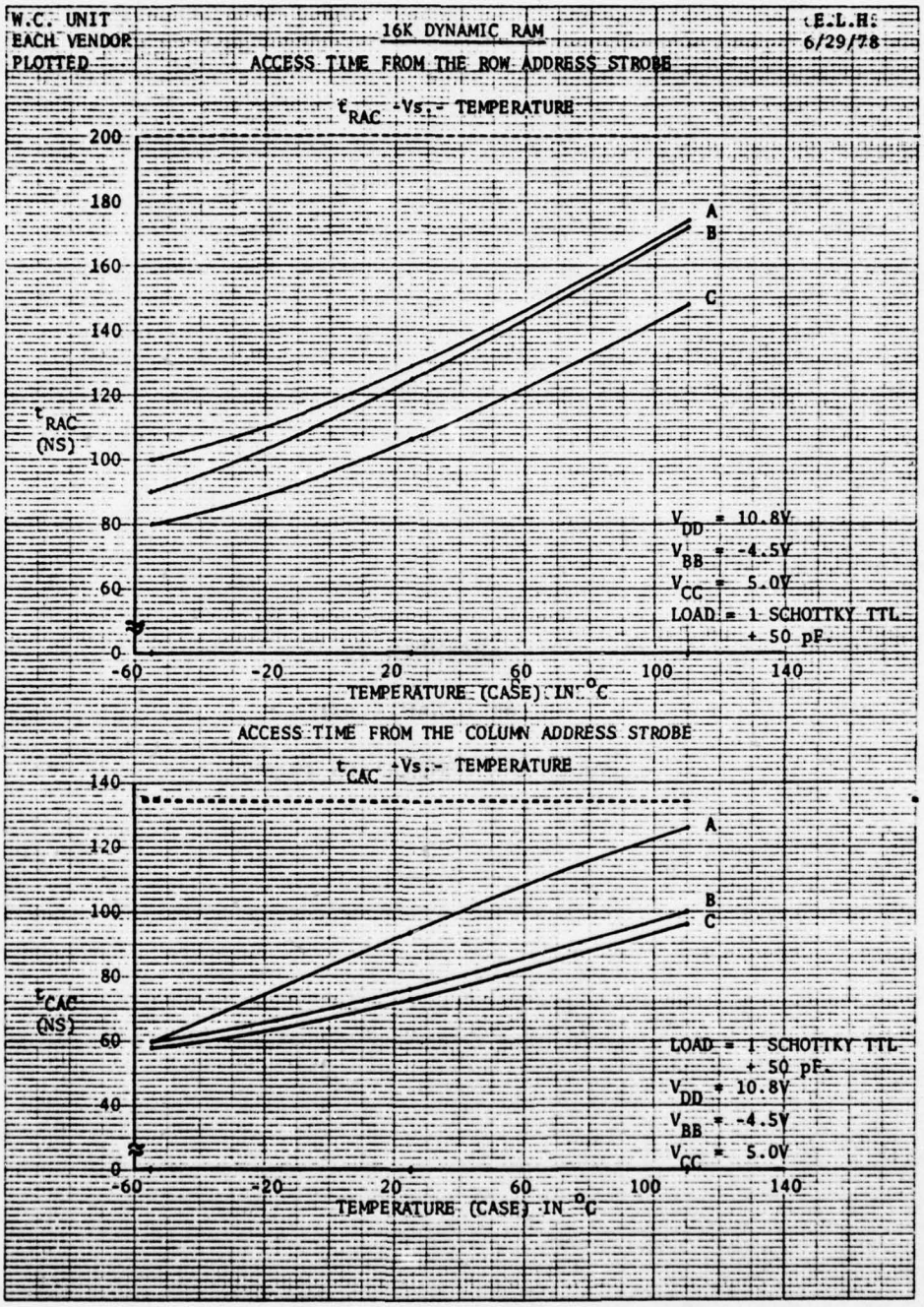
110 °C JUNCTION

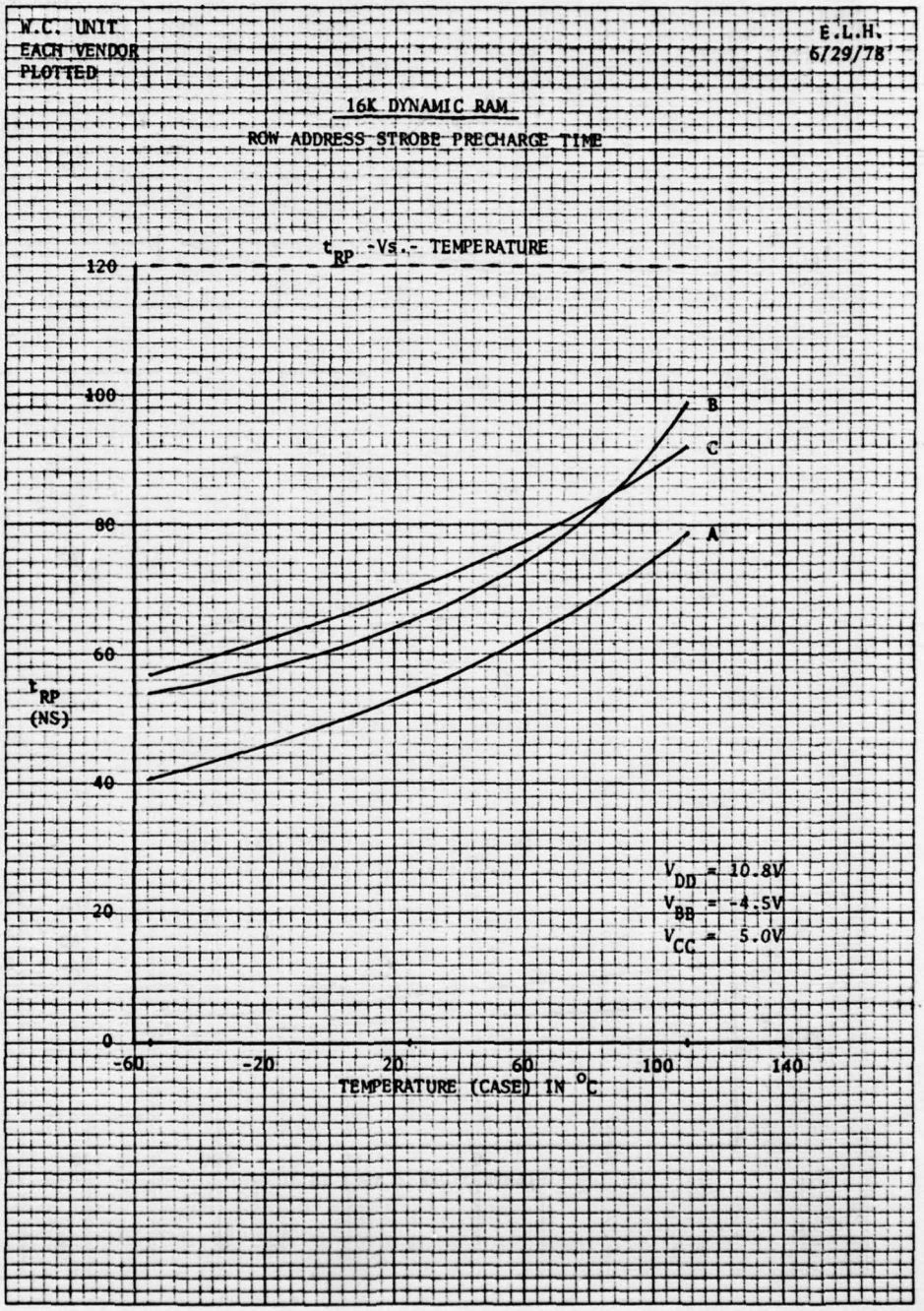


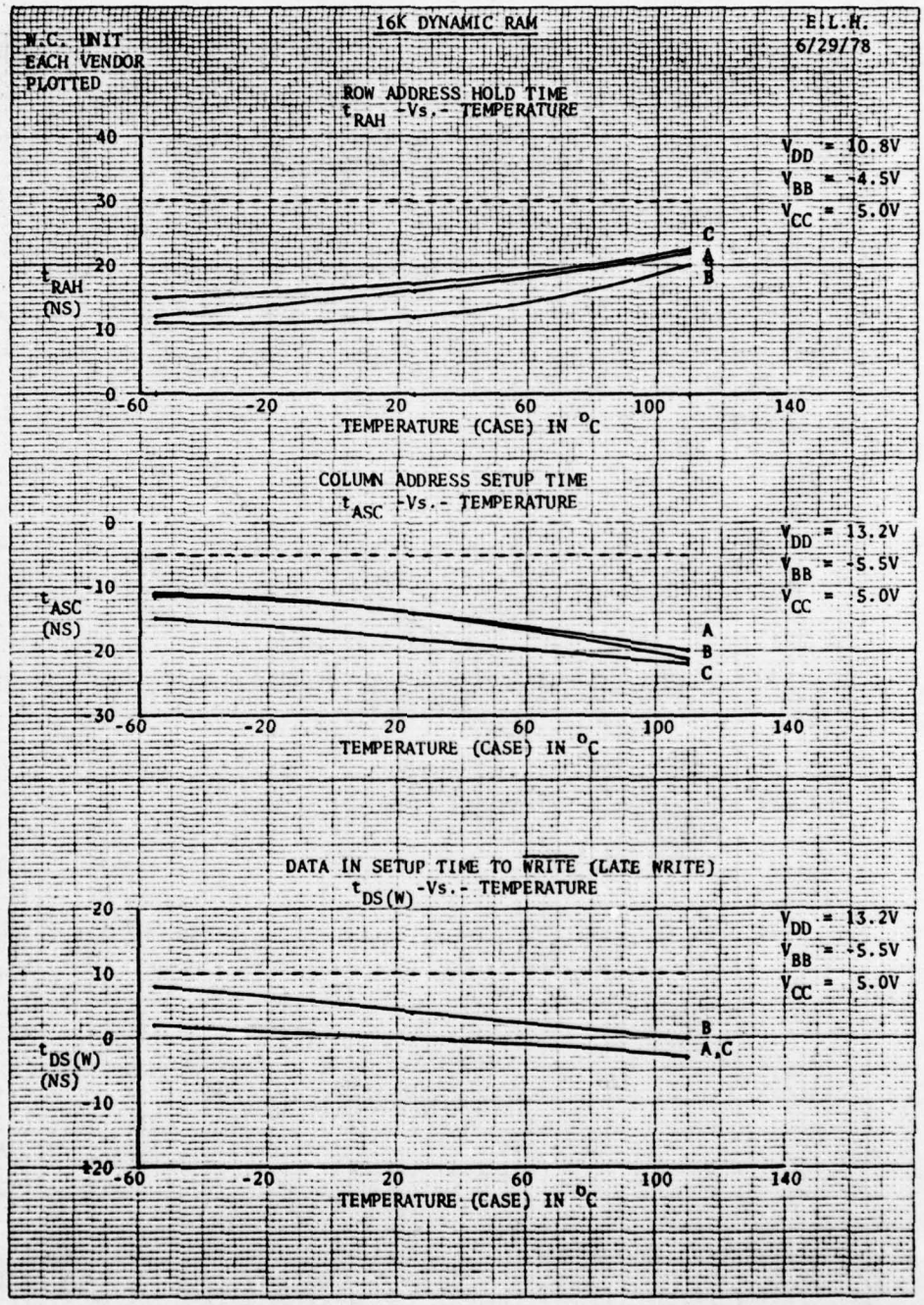
APPENDIX IV

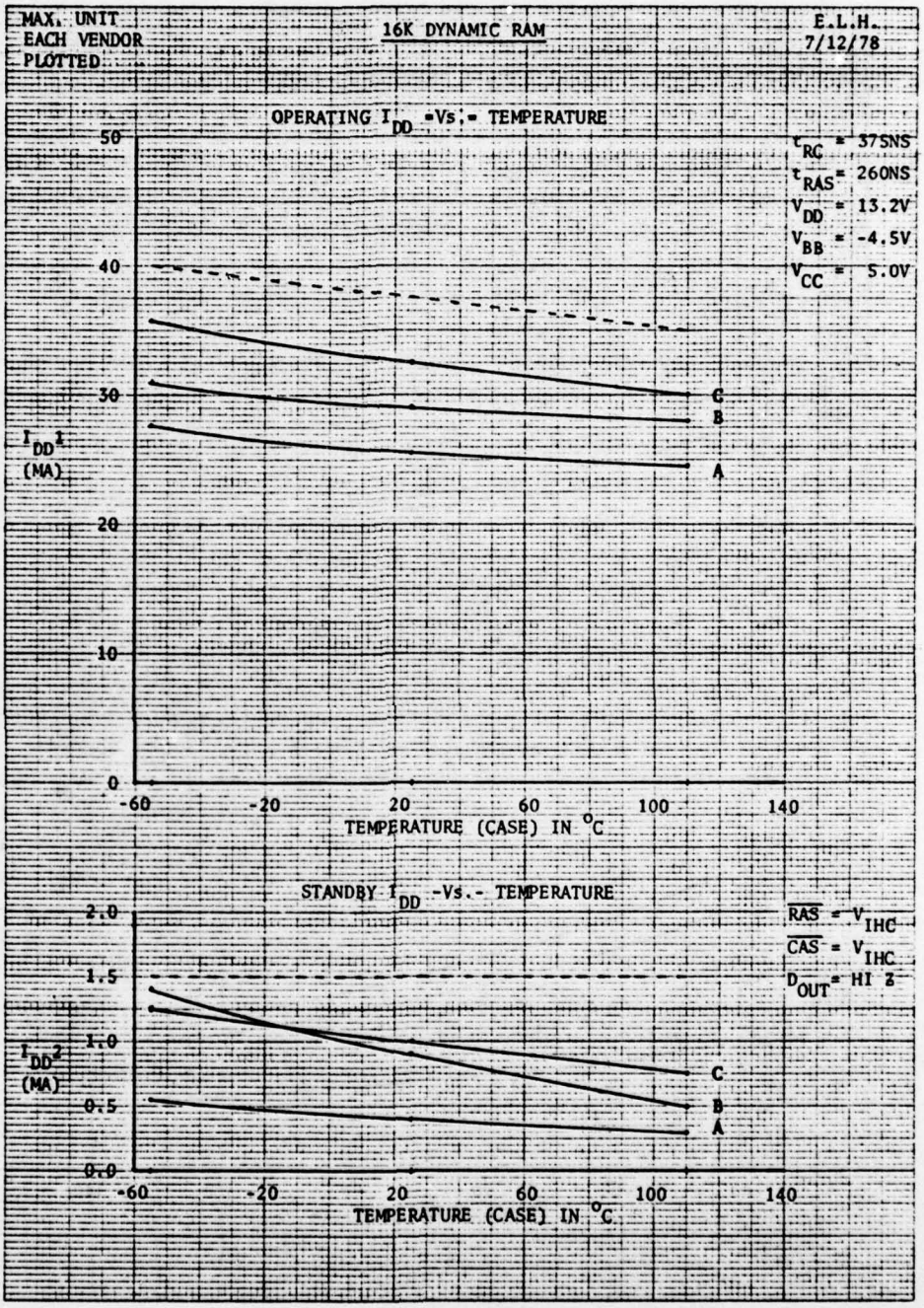
16K DYNAMIC RAM

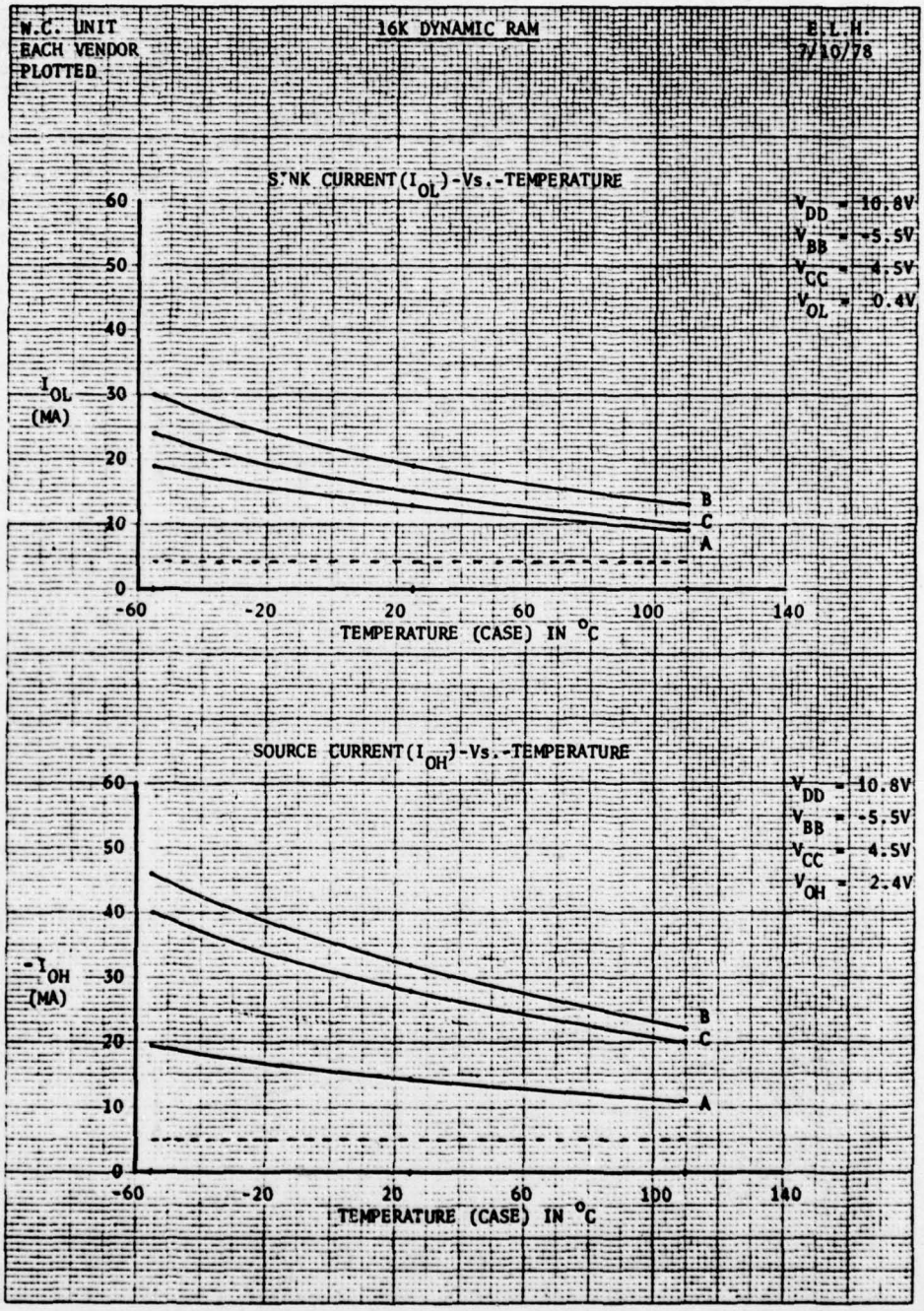
PARAMETER COMPARISON PLOTS


W.C. UNIT
EACH VENDOR
PLOTTED
16K DYNAMIC RAM
E.L.H.
6/29/78
ACCESS TIME FROM THE ROW ADDRESS STROBE
t_{RAC} -Vs.- TEMPERATURE
t_{RAC} (NS)
200
180
160
140
120
100
80
60
0
A
B
C
V_{DD} = 10.8V
V_{BB} = -4.5V
V_{CC} = 5.0V
LOAD = 1 SCHOTTKY TTL
+ 50 pF.
-60
-20
20
60
100
140
TEMPERATURE (CASE) IN °C
ACCESS TIME FROM THE COLUMN ADDRESS STROBE
t_{CAC} -Vs.- TEMPERATURE
t_{CAC} (NS)
140
120
100
80
60
40
0
A
B
C
LOAD = 1 SCHOTTKY TTL
+ 50 pF.
V_{DD} = 10.8V
V_{BB} = -4.5V
V_{CC} = 5.0V
-60
-20
20
60
100
140
TEMPERATURE (CASE) IN °C


N.C. UNIT
EACH VENDOR
PLOTTED
E.L.H.
6/29/78
16K DYNAMIC RAM
ROW ADDRESS STROBE PRECHARGE TIME
t_{RP} -Vs.- TEMPERATURE
120
100
80
60
40
20
0
t_{RP}
(NS)
B
C
A
V_{DD} = 10.8V
V_{BB} = -4.5V
V_{CC} = 5.0V
-60
-20
20
60
100
140
TEMPERATURE (CASE) IN °C


16K DYNAMIC RAM
E.I.L.H.
6/29/78
W.C. UNIT
EACH VENDOR
PLOTTED
ROW ADDRESS HOLD TIME
t_{RAH} -Vs.- TEMPERATURE
V_{DD} = 10.8V
V_{BB} = -4.5V
V_{CC} = 5.0V
t_{RAH} (NS)
40
30
20
10
0
C
A
B
-60
-20
20
60
100
140
TEMPERATURE (CASE) IN °C
COLUMN ADDRESS SETUP TIME
t_{ASC} -Vs.- TEMPERATURE
V_{DD} = 13.2V
V_{BB} = -5.5V
V_{CC} = 5.0V
t_{ASC} (NS)
0
-10
-20
-30
A
B
C
-60
-20
20
60
100
140
TEMPERATURE (CASE) IN °C
DATA IN SETUP TIME TO WRITE (LATE WRITE)
$t_{DS(W)}$ -Vs.- TEMPERATURE
V_{DD} = 13.2V
V_{BB} = -5.5V
V_{CC} = 5.0V
$t_{DS(W)}$ (NS)
20
10
0
-10
-20
B
A,C
-60
-20
20
60
100
140
TEMPERATURE (CASE) IN °C


MAX. UNIT EACH VENDOR PLOTTED
16K DYNAMIC RAM
E.L.H. 7/12/78
OPERATING I_{DD} -Vs.- TEMPERATURE
t_{RC} = 375NS
t_{RAS} = 260NS
V_{DD} = 13.2V
V_{BB} = -4.5V
V_{CC} = 5.0V
$I_{DD}1$ (MA)
50
40
30
20
10
0
C
B
A
-60
-20
20
60
100
140
TEMPERATURE (CASE) IN °C
STANDBY I_{DD} -Vs.- TEMPERATURE
$\overline{RAS}$ = V_{IHC}
$\overline{CAS}$ = V_{IHC}
D_{OUT} = HI Z
$I_{DD}2$ (MA)
2.0
1.5
1.0
0.5
0.0
C
B
A
-60
-20
20
60
100
140
TEMPERATURE (CASE) IN °C


N.C. UNIT
EACH VENDOR
PLOTTED
16K DYNAMIC RAM
E.L.H.
7/10/78
SINK CURRENT (I_{OL})-Vs.-TEMPERATURE
V_{DD} = 10.8V
V_{BB} = -5.5V
V_{CC} = 4.5V
V_{OL} = 0.4V
I_{OL} (MA)
60
50
40
30
20
10
0
B
C
A
-60
-20
20
60
100
140
TEMPERATURE (CASE) IN °C
SOURCE CURRENT (I_{OH})-Vs.-TEMPERATURE
V_{DD} = 10.8V
V_{BB} = -5.5V
V_{CC} = 4.5V
V_{OH} = 2.4V
$-I_{OH}$ (MA)
60
50
40
30
20
10
0
B
C
A
-60
-20
20
60
100
140
TEMPERATURE (CASE) IN °C

16K DYNAMIC RAM

DEVICE CAPACITANCE

Device input and output capacitance measurements were made using a BOONTON Model 75B-S8 capacitance bridge. This bridge uses a test frequency of 1.0 MHZ. The test signal amplitude was set at 20 MV P-P.

Measurements were made with nominal voltages applied, and taken under biased conditions. Increasing bias from 0.0V to 2.4V or 2.7V in the case of the clock inputs, increases capacitance by 1.0 to 1.5 pF. The WORSE CASE reading for each input and the data output pin are recorded below.

		VENDOR		
		A	B	C
PIN 2	D_{IN}	= 2.1 pF	1.9 pF	2.3 pF
PIN 3	$\overline{WRITE}$	= 3.5 pF	2.4 pF	3.1 pF
PIN 4	$\overline{RAS}$	= 4.0 pF	3.4 pF	3.8 pF
PIN 5	A_0	= 2.0 pF	2.1 pF	1.8 pF
PIN 6	A_2	= 1.8 pF	2.1 pF	1.5 pF
PIN 7	A_1	= 1.9 pF	1.9 pF	1.6 pF
PIN 10	A_5	= 2.0 pF	2.3 pF	1.9 pF
PIN 11	A_4	= 1.9 pF	2.0 pF	1.5 pF
PIN 12	A_3	= 2.1 pF	2.1 pF	1.8 pF
PIN 13	A_6	= 2.2 pF	2.7 pF	1.8 pF
PIN 14	D_{OUT}	= 2.8 pF	2.7 pF	2.8 pF
PIN 15	$\overline{CAS}$	= 4.3 pF	5.0 pF	5.4 pF

APPENDIX V

16K DYNAMIC RAM

RECOMMENDED PARAMETER LIMITS

16K DYNAMIC RAM REV. G DATE CODE 7751

A.C. CHARACTERIZATION DATA OVERVIEW

PARAMETER	SYMBOL	-55°C TYP.	-55°C W.C.	25°C TYP.	25°C W.C.	110°C TYP.	110°C W.C.	UNITS	RADC PROP.LIM.	P.S. Cond.
Random Read or Write Cycle Time	t_{RC}	IN ORDER TO SET CHIP TEMPERATURE						NS	375Min	
Read-Write Cycle Time	t_{RWC}	LIMITS, A MINIMUM CYCLE TIME,AS						NS	375Min	
Page Mode Cycle Time	t_{PC}	SPECIFIED IN PROPOSED LIMITS WAS USED						NS	225Min	
Access Time from $\overline{RAS}$	t_{RAC}	96	100	114	129	155	174	NS	200Max	1
Access Time from $\overline{CAS}$	t_{CAC}	54	60	71	94	97	126	NS	135Max	1
Output buffer turn-off delay	t_{OFF}	21	22	25	25	28	30	NS	50Max	2
Output buffer turn-off delay	t_{OFF}	21	16	25	21	28	25	NS	0Min	1
$\overline{RAS}$ precharge time	t_{RP}	30	41	42	56	55	79	NS	120Min	1
$\overline{RAS}$ pulse width	t_{RAS}	76	87	100	112	132	150	NS	200Min	1
$\overline{RAS}$ pulse width	t_{RAS}	PASSED SCREEN AT 10.0 US						US	10Max	
$\overline{RAS}$ hold time	t_{RSH}	48	56	61	70	78	92	NS	135Min	1
$\overline{CAS}$ hold time	t_{CSH}	118	125	135	143	156	172	NS	200Min	
$\overline{CAS}$ pulse width	t_{CAS}	53	60	70	78	91	107	NS	135Min	1
$\overline{CAS}$ pulse width	t_{CAS}	PASSED SCREEN AT 10.0 US						US	10Max	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	10.5	12	14	16	16.5	22	NS	25Min	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	-	132	-	106	-	74	NS	65Max	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	≤ -50 over temp. range						NS	-20Min	
Row address set-up time	t_{ASR}	-6	-2	-9	-6	-10	-9.5	NS	0Min	2
Row Address hold time	t_{RAH}	10.5	12	14	16	16.5	22	NS	25Min	1
Column Address set-up time	t_{ASC}	-14	-11	-18	-14	-25	-20	NS	-10Min	2
Column Address hold time	t_{CAH}	-	30	-	-	-	40	NS	55Min	1
Column Address hold time referenced to $\overline{RAS}$	t_{AR}	-	95	-	-	-	105	NS	120Min	1
Read command set-up time	t_{RCS}	-22	-19	-29	-25	-39	-33	NS	0Min	2
Read command hold time	t_{RCH}	assed a-1NS Screen over Temperature						NS	0Min	
Write command hold time	t_{WCH}	24	28	32	38	42	52	NS	55Min	1
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	52	61	70	79	90	104	NS	120Min	1
Write command pulse width	t_{WP}	11	12	16	19	19	25	NS	55Min	1
Write command to $\overline{RAS}$ lead time	t_{RWL}	13	19	18	25	24	35	NS	80Min	1
Write command to $\overline{CAS}$ lead time	t_{CWL}	13	16	18	24	25	36	NS	80Min	1
Data-in set-up time to $\overline{CAS}$	$t_{DS(C)}$	-10	- 7	-16	-12	-24	-19	NS	0Min	2
Data-in set-up time to $\overline{WRITE}$	$t_{DS(W)}$	+ 1	+ 2	- 2	0	- 5	- 3	NS	10Min	1
Data-in hold time to $\overline{CAS}$	$t_{DH(C)}$	17	21	23	27	31	36	NS	60 Min	1
Data-in hold time to $\overline{WRITE}$	$t_{DH(W)}$	9	11	11	14	14	18	NS	60 Min	1
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	51	57	63	72	84	101	NS	125 Min	1
$\overline{CAS}$ precharge time(Page-mode only)	t_{CP}	-	20	-	-	-	30	NS	80Min	
Refresh period	t_{REF}	RANGE of 2.15 to 7.3 @ 110°C(CASE)						MS	1.0Max	3
WRITE command set-up time	t_{WCS}	-41	-36	-51	-46	-62	-56	NS	-20Min	2
$\overline{CAS}$ to $\overline{WRITE}$ delay	t_{CWD}	42	48	52	58	64	73	NS	95Min	1
$\overline{RAS}$ to $\overline{WRITE}$ delay	t_{RWD}	70	79	92	101	120	131	NS	160Min	3

Temperatures are CASE

TYP.=All Voltages NOMINAL
W.C.=Voltages Worse Case by ± 10%

P.S. Cond. 1=V_{DD}=10.8V,V_{BB}=-4.5V,V_{CC}=5.0V

P.S. Cond. 2=V_{DD}=13.2V,V_{BB}=-5.5V,V_{CC}=5.0V

P.S. Cond. 3=V_{DD}=10.8V,V_{BB}=-5.5V,V_{CC}=5.0V

Above data taken with transition times (tT Rise and Fall) of 3-5NS

Input Levels: Vihc:2.7v,Vih=2.4v,Vil=0.8v
measurement points were 1.5v to 1.5v levels

16K DYNAMIC RAM REV. G DATE CODE 7751

D.C. CHARACTERIZATION DATA OVERVIEW

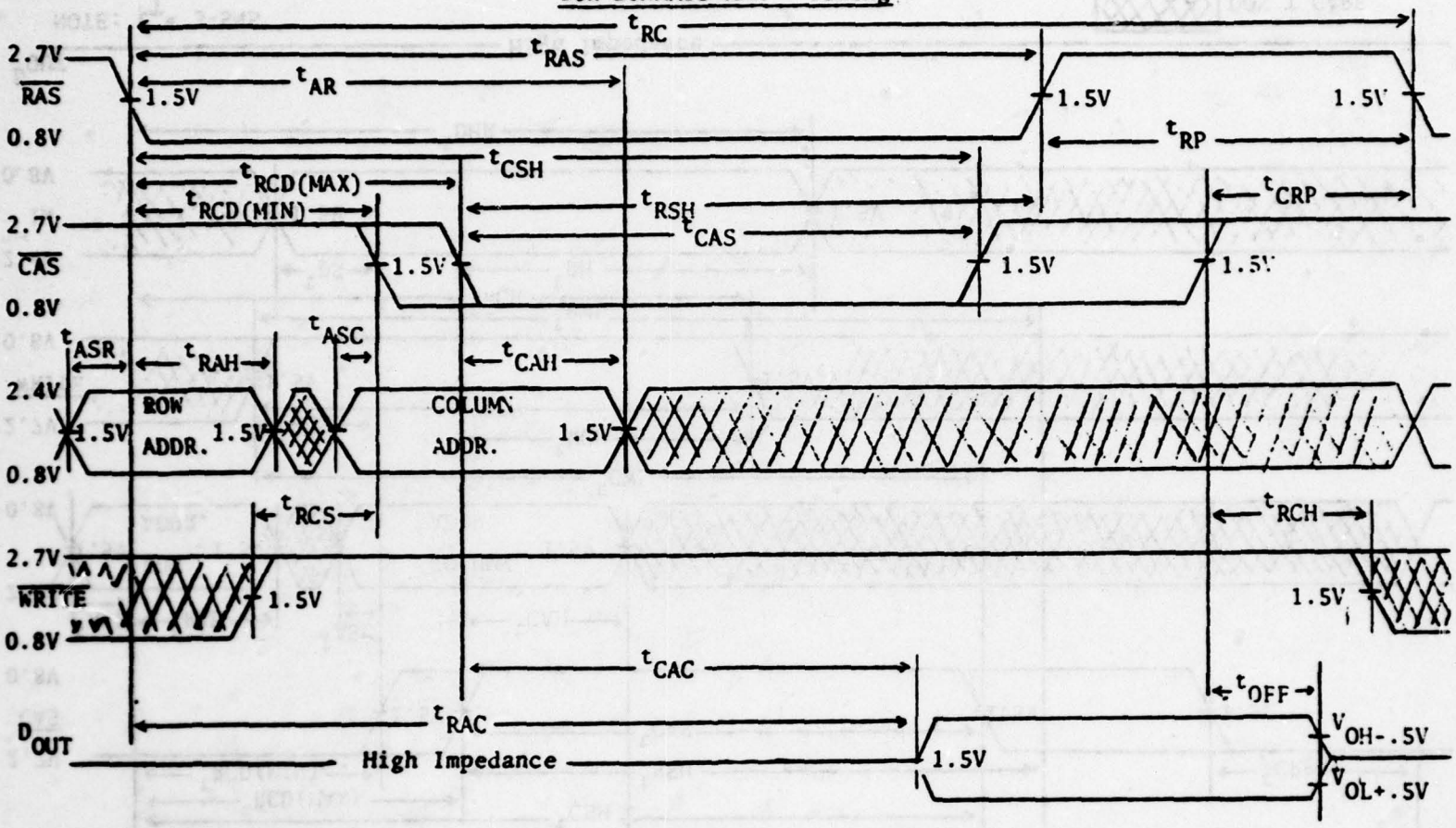
PARAMETER	SYMBOL	-55°C TYP.	-55°C W.C.	25°C TYP.	25°C W.C.	110°C TYP.	110°C W.C.	UNITS	RADC PROP.LIM.	P.S. COND.	NOTES
OPERATING CURRENT	$I_{DD\ 1}$	23.3	27.4	22.0	25.5	21.0	24.4	MA	40Max	2	1
$\overline{RAS}$, $\overline{CAS}$ CYCLING	$I_{CC\ 1}$	-	149	-	151	-	154	µA	600Max	1	2
t_{RC}=375NS	$I_{BB\ 1}$	98	249	49	120	29	73	µA	400Max	2	
STANDBY CURRENT	$I_{DD\ 2}$	0.47	0.54	0.33	0.39	0.23	0.29	µA	1.5Max	2	
$\overline{RAS}$, $\overline{CAS}$=V_{IHC}	$I_{CC\ 2}$	-	-	-	-	-	-	µA	10Max		
D_{OUT}=HIGH IMPEDANCE	$I_{BB\ 2}$	0.8	1.5	0.5	0.5	1.0	1.0	µA	100Max	2	
REFRESH CURRENT	$I_{DD\ 3}$	15.3	15.8	14.3	14.7	13.6	14.0	µA	27Max	2	1
$\overline{RAS}$ CYCLING t_{RC}=375NS	$I_{CC\ 3}$	-	-	-	-	-	-	µA	10Max		
$\overline{CAS}$=V_{IHC}	$I_{BB\ 3}$	SEE $I_{BB\ 1}$						µA	400Max	2	
PAGE MODE CURRENT	$I_{DD\ 4}$	PAGE MODE NOT TESTED						MA	27Max	2	1
$\overline{RAS}$=V_{IL} $\overline{CAS}$ CYCLING	$I_{CC\ 4}$	PROPOSED LIMITS GUARANTEED						µA	1000Max	1	2
t_{PC}=225NS	$I_{BB\ 4}$							µA	400Max	2	
INPUT HIGH VOLTAGE	V_{IHC}	-	-	-	-	-	-	V	7.0Max		
$\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$		1.84	1.82	1.66	1.76	1.56	1.65	V	2.7Min	4	
INPUT HIGH VOLTAGE	V_{IH}	-	-	-	-	-	-	V	7.0Max		
A0-A6, D_{IN}		1.82	2.0	1.72	1.9	1.62	1.8	V	2.4Min	4	
INPUT LOW VOLTAGE	V_{IL}	-	-	-	-	-	-	V	-1.0Min		
ALL INPUTS		1.52	1.42	1.38	1.28	1.24	1.1	V	0.8Max	5	
INPUT LEAKAGE	$I_{I(L)}$	NO DISCERNIBLE LEAKAGE WAS MEASURABLE ON TEKTRONIX TYPE 576 CURVE TRACER (10 NANOAMP RANGE)						µA	-10Min		
								µA	+10Max		
OUTPUT LEAKAGE	$I_{O(L)}$							µA	-10Min		
								µA	+10Max		
OUTPUT HIGH VOLTAGE I_{OUT}=-5.0MA	V_{OH}	3.5	3.4	3.7	3.6	4.0	3.9	V	2.4Min	3	
OUTPUT LOW VOLTAGE I_{OUT}=4.2MA	V_{OL}	-	0.09	-	0.13	-	0.19	V	0.4Max	3	
INPUT CAPACITANCE A0-A6, D_{IN}	C_{11}	-	-	-	2.2	-	-	pFd	5Max	NOMINAL	3
INPUT CAPACITANCE $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{12}	-	-	-	4.3	-	-	pFd	10Max	NOMINAL	3
OUTPUT CAPACITANCE	C_O	-	-	-	2.8	-	-	pFd	7Max	NOMINAL	3

TEMPERATURES ARE CASE
TYP.=ALL VOLTAGES NOMINAL
W.C.=VOLTAGES WORSE CASE (SEE P.S. COND.)

P.S. COND.
1 V_{DD}=10.8V, V_{BB}=-4.5V, C_{CO}=5.5V
2 V_{DD}=13.2V, V_{BB}=-4.5V, V_{CC}=5.0V
3 V_{DD}=10.8V, V_{BB}=-5.5V, V_{CC}=4.5V
4 V_{DD}=13.2V, V_{BB}=-5.5V, V_{CC}=5.0V
5 V_{DD}=10.8V, V_{BB}=-4.5V, V_{CC}=5.0V

NOTES:
1) DEPENDS ON CYCLE RATE
2) DEPENDS ON OUTPUT LOAD. (ONE SCHOTTKY TTL + 50pFd) ALTERNATING "1", "0" PATTERN IS WORSE CASE.
3) MEASUREMENTS MADE USING A BOONTON MOD 75B-S8 CAPACITANCE BRIDGE, 1.0MHZ, 20MV P-P.

16K DYNAMIC RAM - Timing

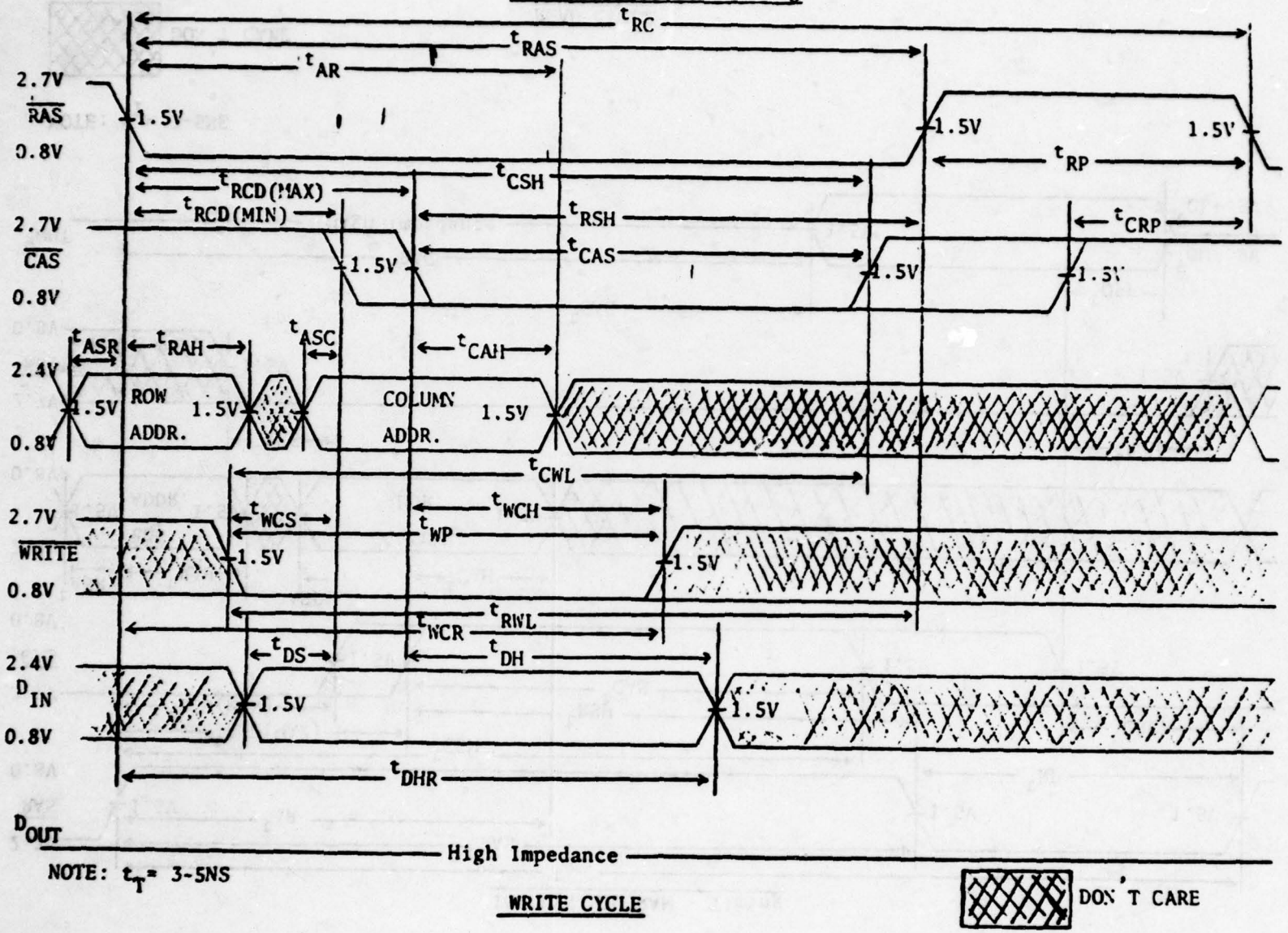


NOTE: t_T = 3-5NS

DON'T CARE

READ CYCLE

16K DYNAMIC RAM - Timing



WRITE CYCLE

APPENDIX VI

16K DYNAMIC RAM

TEST ALGORITHMS

NOTE: The tests described here-in were used for characterization only and in no way reflect what should or should not be used for production testing.

16K DYNAMIC RAM

Pattern 1 - Address Complement, Data Background = Y-BAR

This pattern produces a checkerboard and its complement in an inter-digited array. It produces maximum address line noise and checks the decoder dynamic response times. It is performed in the following manner.

Step 1 - Perform 8 pump cycles
Step 2 - Load memory with background data
Step 3 - Read entire memory (DATA Verification)
Step 4 - Read minimum address location
Step 5 - Read maximum address location
Step 6 - Read location min. +1
Step 7 - Read location max. -1
Step 8 - Continue incrementing and decrementing from min. and max. locations until all locations have been read
Step 9 - Repeat steps 2 through 8 with complement data

Test Time = 3N x cycle time + 8 cycles

Pattern 2 - Shifting Diagonal, Initial Data Background = Major Diagonal

This pattern is a good test for sense line imbalance and response plus restore noise in addition to multiple selection. It is performed in the following manner.

Step 1 - Perform 8 pump cycles
Step 2 - Load memory with data background, scan from minimum location to maximum location
Step 3 - Read data in the memory, scan from maximum location to minimum location
Step 4 - Repeat steps 2 and 3, each time shifting the diagonal by one until it has occupied every position in the memory (128 Load/Read scans)
Step 5 - Repeat steps 2 through 4 with complement data

Test Time = 256N x cycle time + 8 cycles

Pattern 3 - March Data, Data Background = All "0"

This pattern tests for address uniqueness and multiple selection. It is performed in the following manner.

Step 1 - Perform 8 pump cycles
Step 2 - Load memory with background data
Step 3 - Read location 0
Step 4 - Write data complement in location 0
Step 5 - Read data complement in location 0
Step 6 - Repeat steps 3 through 5 for all other locations in the memory (sequentially)
Step 7 - Read data complement at MAX. location
Step 8 - Write data at MAX. location
Step 9 - Read data at MAX. location
Step 10 - Repeat steps 7 through 9 for all other locations in the memory (decrementing from MAX. location to MIN. location)
Step 11 - Repeat steps 3 through 10 with data background of all "1"

Test Time = 14N x cycle time + 8 pump cycles

Pattern 4 - Static Refresh (Periphery Retention)

This pattern tests for periphery retention time by attempting to write after a lengthy pause. This test is performed at 110°C (CASE) only and is not used to measure the retention time of the periphery circuits but to ensure that they will hold for at least 5 MS. It is performed in the following manner.

Step 1 - Perform 8 pump cycles
Step 2 - Load memory with all "0"s
Step 3 - Read memory, all "0"s
Step 4 - Pause (stop all clocks) 5 MS
Step 5 - Load memory with all "1"s
Step 6 - Read memory, all "1"s
Step 7 - Pause (stop all clocks) 5 MS
Step 8 - Load memory with all "0"s
Step 9 - Read memory, all "0"s

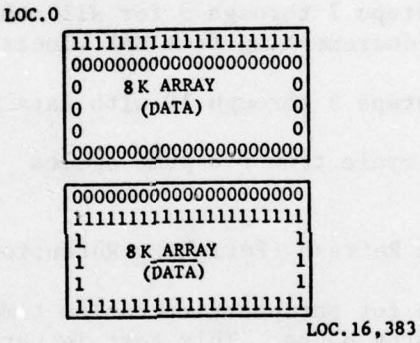
Test Time = 6N x cycle time + 8 cycles + 10 MS

Pattern 5 - Refresh Test (Cell Retention)

This test is used to check the retention time of the memory cells under dynamic conditions. It is done at high temperatures only and is performed in the following manner.

Step 1 - Perform 8 pump cycles
Step 2 - Load memory with DATA as shown below
Step 3 - Read entire memory (DATA verification)
Step 4 - Alternate reading between LOC. 63 and LOC. 64*
Step 5 - Read entire memory
Step 6 - Load memory with $\overline{\text{DATA}}$
Step 7 - Repeat steps 3 through 5

* Refresh (t_{REF}) = # reads x cycle time



NOTE: DATA is not complemented on A_6

Pattern 6 - Extended Cycle Test (10 μs), Data Background = X-BAR

This test is used to verify the 10 μs max limit on $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ pulse width. Front and back edge timing is held to normal cycle timing while the cycle is increased to allow 10 μs of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active time (low level). It is performed in the following manner.

Step 1 - Perform 8 pump cycles
Step 2 - Write data in location 0
Step 3 - Read data in location 0
Step 4 - Repeat steps 2 and 3 for all other locations in the memory (sequentially)
Step 5 - Repeat steps 2 through 4 with complement data.

Test Time = 4N x cycle time + 8 pump cycles

Pattern 7 - Continuous Read, Data Background = X-BAR

This pattern is used to allow the maximum amount of current (I_{CC}) to be drawn from the V_{CC} power supply. It is performed in the following manner with normal cycle timing. It also applies to I_{DD} and I_{BB} currents.

Step 1 - Perform 8 pump cycles
Step 2 - Load memory with background data
Step 3 - Sequentially read entire memory
Step 4 - Repeat step 3 as many times as necessary to achieve a stabilized current reading

Test Time - Undefined

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